INSTRUCTION MANUAL

FOR

WJ-8718/488-2 OPTION

WATKINS-JOHNSON

INSTRUCTION MANUAL

FOR

WJ-8718/488-2 OPTION

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7/85

WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equipment with any of the protective covers removed.

TABLE OF CONTENTS

GENERAL DESCRIPTION

Paragraph		Page
1.1	General Description	1-1
1.2	Mechanical Description	1-1
1.2.1	Equipment Supplied	1-1
1.2.2	Equipment Required But Not Supplied	1-1

INSTALLATION PROCEDURES

1.3	Installation Procedures	1-2
1.3.1	Removing Type 791828 and 791575 Boards From Receiver	1-2
1.3.2	Mounting the WJ-8718/488-2 Components	1-4

OPERATION

1.4	Preparation For Operation	1-4
1.4.1	Remote Operating Mode	1-5
1.4.2	Receiver Address	1-5
1.5	Operation	1-6
1.5.1	488-1975 Interface Bus	1-6
1.5.1.1	Data Lines	1-6
1.5.1.2	Handshake Lines	1-7
1.5.1.3	Management Control Lines	1-9
1.5.2	Parameter Data	1-9
1.5.2.1	Command Data Format	1-12
1.5.2.1.1	Remote Command Programming	1-12
1.5.2.1.2	Remote Monitor Programming	1-14

FUNCTIONAL DESCRIPTION

1.6	Functional Description	1-17
1.6.1	Input/Output Port	1-17
1.6.2	Memory Devices	1-17
1.6.3	Read-Only/Write-Only Devices	1-17
1.6.4	Microprocessor	1-18
1.6.4.1	Registers	1-18
1.6.4.1.1	Program Counter and Stack Pointer	1-18
1.6.4.1.2	Instruction Register and Decoder	1-22
1.6.4.1.3	Arithmetic Logic Unit (ALU) and Flag Register	1-22
1.6.4.2	Internal Clock Generator and Timing	1-23

TABLE OF CONTENTS (Continued)

FUNCTIONAL DESCRIPTION (Continued)

Paragraph		Page
1.6.4.3	Interrupt Control	1-23
1.6.4.4	Data Bus Control Lines ($\overline{RD}$, $\overline{WR}$, ALE)	1-23
1.6.4.5	Reset In/Reset Out	1-25
1.6.5	I/O Interface Board	1-25
1.6.6	IF Interface Board	1-25
1.6.7	Synthesizer Interface Board	1-25

CIRCUIT DESCRIPTION

1.7	Detailed Circuit Description	1-26
1.7.1	Type 794275-X Synthesizer Interface and Memory Board (488-A1)	1-26
1.7.1.1	Microprocessor (U18)	1-26
1.7.1.2	Power Up/Down Circuit (U11)	1-26
1.7.1.3	Read-Only Memory (U1, U2)	1-28
1.7.1.3.1	EPROM Operation	1-28
1.7.1.3.2	Control Inputs	1-29
1.7.1.3.3	Read Mode	1-29
1.7.1.3.4	Standby Mode	1-29
1.7.1.4	Random Access Memory (U3)	1-29
1.7.1.4.1	RAM Operation	1-29
1.7.1.4.2	Control Input	1-30
1.7.1.4.3	Read Mode	1-30
1.7.1.4.4	Write Mode	1-30
1.7.1.4.5	High-Z Mode	1-30
1.7.1.4.6	Low Power Mode	1-30
1.7.1.4.7	Battery Backup	1-30
1.7.1.5	Bidirectional Bus Transceiver (U4)	1-30
1.7.1.6	Address Latch (U5, U6)	1-31
1.7.1.7	Address Decoders (U4, U8)	1-31
1.7.1.8	Frequency Registers (U12-U17)	1-33
1.7.2	Type 794308-1 IF Interface (488-A2)	1-34
1.7.2.1	Bidirectional Bus Transceiver (U20)	1-34
1.7.2.2	Address Latch (U8)	1-34
1.7.2.3	Decoder Select (U11)	1-34
1.7.2.4	Address Decoder (U12)	1-37
1.7.2.5	Frequency Display Register (U4)	1-38
1.7.2.6	Tuning Wheel Register (U17)	1-38
1.7.2.7	Tuning Resolution (U1)	1-41
1.7.2.8	BFO Frequency Buffers (U2, U3)	1-41
1.7.2.9	RF Gain Conversion D/A (U23)	1-42
1.7.2.10	Audio/Gain Switch (U22)	1-42
1.7.2.11	Registers (U5, U9, U21)	1-42

TABLE OF CONTENTS (Continued)

CIRCUIT DESCRIPTION (Continued)

Paragraph		Page
1.7.2.12	Bandwidth, BFO Inhibit, and AGC Dump (U5)	1-43
1.7.2.13	Gain/Detector Mode (U9)	1-44
1.7.2.14	Local/Remote Select (U21B)	1-44
1.7.2.15	AUDIO ON/OFF (U21A, U16A, U16B)	1-44
1.7.2.16	A/D Converter (U25)	1-45
1.7.2.17	Analog Inputs	1-45
1.7.3	Type 796075 I/O Interface (488-A3)	1-46
1.7.3.1	Address Latch (U6)	1-46
1.7.3.2	Address Decoder (U7)	1-46
1.7.3.2.1	U7 Enable	1-46
1.7.3.2.2	U7 Select	1-47
1.7.3.3	Switch Assembly (S1)	1-47
1.7.3.4	Tri-State Buffer/Inverter (U4)	1-48
1.7.3.5	Transceiver Network (U2 and U3)	1-48
1.7.3.6	GPIB (General Purpose Interface Bus), (U1)	1-48
1.7.3.6.1	Read/Write Registers	1-49
1.7.3.6.2	Reset Procedure	1-51
1.7.3.6.3	488 Handshake and Management Signals	1-51
1.7.3.6.4	Direct Memory Access (DMA)	1-51
1.7.3.6.5	Data Ports	1-51
1.7.3.6.6	Clock Input	1-51
1.7.3.6.7	Transmit/Receive Control Lines	1-51
1.7.3.7	Master/Slave Hand Off (U9, U10)	1-52

MAINTENANCE

1.8	Maintenance	1-52
1.8.1	Test Equipment	1-52
1.8.1.1	Logic Probe	1-53
1.8.1.2	Logic Pulser	1-53
1.8.1.3	Current Tracer	1-53
1.8.1.4	Logic Clip	1-53
1.8.2	Performance Tests	1-53
1.8.3	Alignment Procedures	1-54
1.8.3.1	Alignment of Digitized Signal Strength	1-54
1.8.4	Troubleshooting	1-55
1.8.4.1	Symptoms of Integrated Circuit Failure	1-55
1.8.4.2	In-Circuit Tests	1-56
1.8.5	Repair	1-60
1.8.5.1	General Repair Procedure	1-60
1.8.5.2	Removing/Replacing Printed Circuit Components	1-60

TABLE OF CONTENTS (Continued)

PARTS LISTS

Paragraph		Page
1.9	Replacement Parts Lists and Schematic Diagrams	1-60
1.10	Type WJ-8718/488-2 IEEE 488-2 Interface Option	1-63
1.10.1	Type 794275-X Synthesizer Interface and Memory (488-A1)	1-64
1.10.2	Type 794308-1 IF Interface and Memory (488-A2)	1-67
1.10.3	Type 796075 I/O Interface (488-A3)	1-71

LIST OF FIGURES

Figure		Page
1-1	Installation Diagram	1-3
1-2	488 Bus Structure and Interface Block Diagram	1-8
1-3	Handshake Sequence Timing Diagram	1-9
1-4	Data Transfer Timing Diagram	1-11
1-5	WJ-8718/488-2 Option Block Diagram	1-19
1-6	Intel 8085A Microprocessor Block Diagram	1-21
1-7	$\overline{RD}$ Timing Diagram	1-24
1-8	$\overline{WR}$ Timing Diagram	1-24
1-9	Synthesizer Interface and Memory Board, Simplified Block Diagram	1-27
1-10	IF Interface Board, Simplified Block Diagram	1-35
1-11	Timing Diagram for Tuning Wheel Clockwise Rotation	1-40
1-12	Timing Diagram for Tuning Wheel Counterclockwise Rotation	1-41
1-13	GPIB Interface (U1) Block Diagram	1-49
1-14	Signal Strength Alignment Equipment Setup	1-55
1-15	WJ-8718/488-2 Option Troubleshooting Tree	1-57
1-16	Type 794275-X Synthesizer Interface/Memory (488-A1), Location of Components	1-66
1-17	Type 794308-1 IF Interface (488-A2), Location of Components	1-70
1-18	Type 796075 I/O Interface (488-A3), Location of Components	1-72
1-19	Type 794275-X Synthesizer Interface (488-A1), Schematic Diagram 570208	1-75
1-20	Type 794308-1 IF Interface (488-A2), Schematic Diagram 570239	1-77
1-21	Type 796075 I/O Interface (488-A3), Schematic Diagram 480096	1-79
1-22	WJ-8718/488-2 Option, Schematic Diagram 480115	1-81

LIST OF TABLES

Table		Page
1-1	Installation Hardware	1-2
1-2	Receiver Address Codes	1-5

LIST OF TABLES (Continued)

Table		Page
1-3	488 Connector Pin Assignments	1-7
1-4	Register Address Data	1-10
1-5	Decimal Entries for Registers 0 through 7	1-13
1-6	Monitor Program	1-16
1-7	RAM/EPROM Address Data	1-28
1-8	U7 Truth Table	1-31
1-9	U8 Truth Table	1-32
1-10	Addresses 1030 through 1035	1-32
1-11	RF Frequency Data Words	1-33
1-12	BFO Frequency Data Words	1-33
1-13	Addresses 1010 through 1017	1-36
1-14	Addresses 1035 through 1037	1-36
1-15	U11 Truth Table	1-37
1-16	U12 Truth Table	1-37
1-17	Frequency Display Data Word	1-38
1-18	U17 Truth Table	1-39
1-19	Bandwidth Code	1-43
1-20	Address 1011 (U5) Data Word	1-43
1-21	Address 1012 (U9) Data Word	1-44

1.1 GENERAL DESCRIPTION

The WJ-8718/488-2 Option, when installed in the WJ-8718 HF Receiver, permits integration of the receiver with remote control equipment that is compatible with the IEEE Standard 488-1975 format. Up to 14 WJ-8718 HF Receivers, equipped with the option, can be addressed to receive or transmit (Listen/Talk) by one controller, via the 488-1975 bus. The bus structure is designed around a three-line handshake circuit which permits asynchronous communication with devices that assimilate data at different rates. A bit-parallel, byte-serial, negative logic form is used for the bidirectional transfer of data between the remote control equipment and the receiver under control.

The receiver control block is built around an 8-bit parallel microprocessor. Inputs to the control block consist of encoded data from the front panel controls or from an external source, via the receiver rear panel REMOTE INPUT. The control block processes the encoded inputs and develops data which are used to drive the synthesizer, IF, gain mode, and demodulator circuits in the receiver.

Receiver parameters that can be controlled and monitored are tuned and BFO frequencies, detection mode, gain mode, and IF bandwidth. RF gain is controlled in the receiver manual gain mode, via remote control in a command sequence. Signal strength is monitored when the receiver is requested to transmit.

1.2 MECHANICAL DESCRIPTION

The WJ-8718/488-2 Option for the WJ-8718 HF Receiver consists of three printed circuit boards mounted by edge connectors to the receiver's I/O Motherboard, A6. The 488-A1 board replaces the receiver's Manual Tuning Up/Down Counter Board, A6A1; the 488-A2 board replaces the Front Panel Interconnect Board, A6A2. The 488-A3 board is connected to the receiver rear panel REMOTE INPUT, a 24-pin amphenol receptacle which accepts the bus cable from the controller. Multiconductor cables provide the connection to the REMOTE INPUT and to the interboard wiring.

The maximum accumulative length of the bus cable in any system must not exceed more than 2 meters per receiver (up to 16) or 20 meters, whichever is less.

1.2.1 EQUIPMENT SUPPLIED

The WJ-8718/488-2 Option consists of three printed circuit boards: Type 794275-X Synthesizer Interface Board (488-A1); Type 794308-1 IF Interface Board (488-A2); and Type 796075 I/O Interface (488-A3). Interconnect cables (W1 and W2) and hardware required for installing the option in the receiver (**Table 1-1**) are also supplied.

1.2.2 EQUIPMENT REQUIRED BUT NOT SUPPLIED

To remotely control and monitor the WJ-8718/488-2 Option equipped receiver, a control unit compatible with the IEEE 488-1975 bus is required. The Hewlett-Packard 9825A Calculator is a typical control unit and is referenced as an example in this manual.

Table 1-1. Installation Hardware

Quantity	Item	Part Number
2	Phillips-Head Screw	S260047
2	Lockwasher	S140257
2	Hex Nut	S260125
2	Washer	S140159

1.3 INSTALLATION PROCEDURES

The following procedures outline the WJ-8718 HF Series Receiver modifications and the WJ-8718/488-2 assembly and mounting instructions. **Figure 1-1**, the WJ-8718/488-2 Installation Diagram, should be referred to as necessary.

1.3.1 REMOVING TYPE 791828 AND 791575 BOARDS FROM RECEIVER

1. Remove power from the receiver.

2. Loosen the 34 quarter-turn fasteners securing the receiver top cover and lift the cover from the receiver.

3. In the receiver, locate the Type 791828, Front Panel Interconnect Assembly, A6A2.

4. Loosen the A6A2 board and lift it to the top of the receiver. Remove cable connector A10P1 from right angle board connector, J1. Remove the A6A2 board from the receiver.

5. In the receiver, locate the Type 791575-1 or 791575-2, Manual Tuning Up/Down Counter Assembly, A6A1. If the assembly is Type 791575-2, perform steps 6 and 7 of the following procedure; if the assembly is Type 791575-1, omit step 6 and perform step 7 only.

6. Remove cable connector A6A1J1 from the rear panel location marked REMOTE INPUT, by removing the two nuts, lockwashers, flatwashers, and screws that secure the A6A1J1 connector.

7. Loosen the A6A1 board and lift it to the top of the receiver. Remove cable connector A8P1 from J2, A9P1 from J3, and A7A1P1 from J4. Remove the board from the receiver.

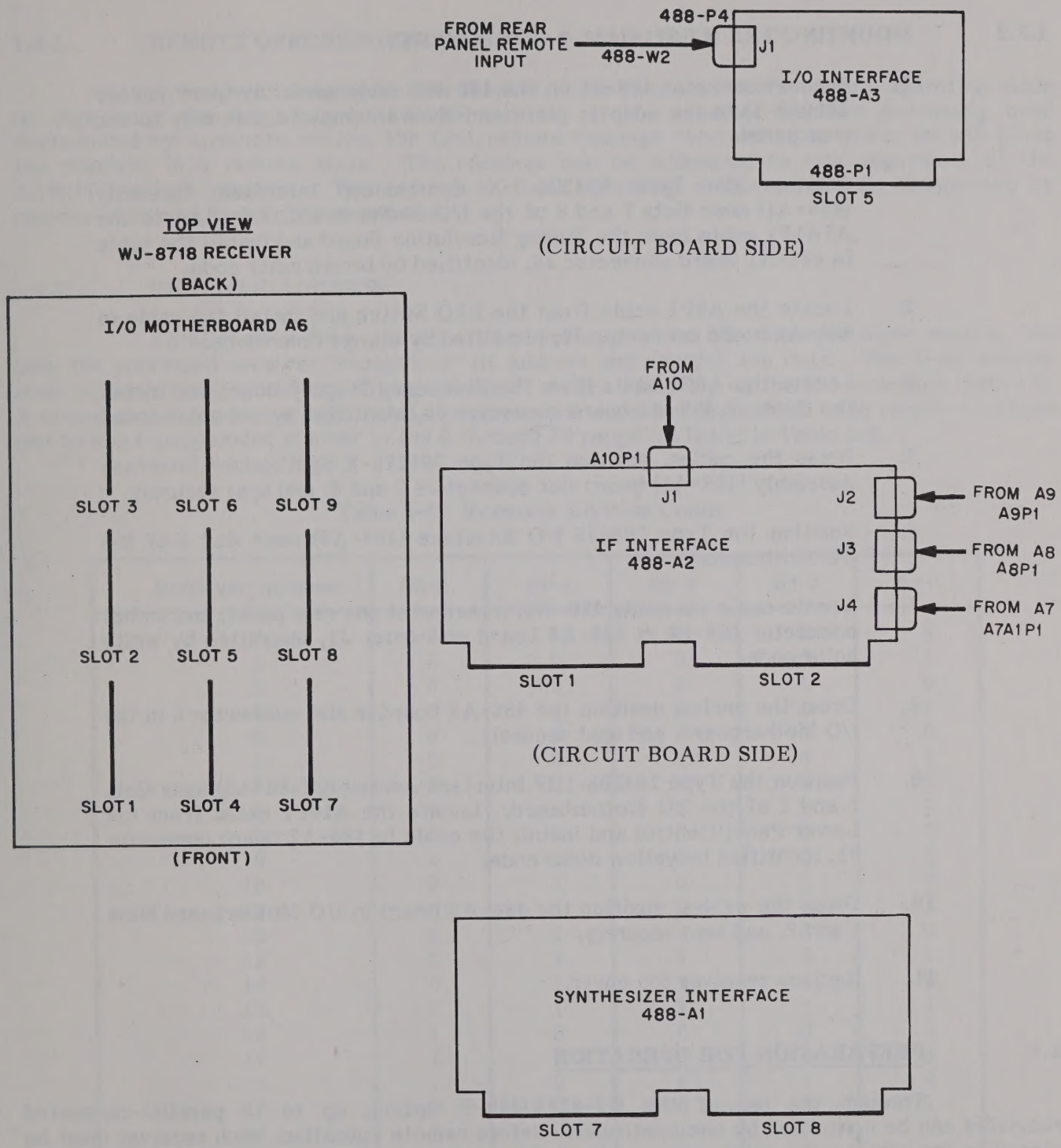

Figure 1-1. Installation Diagram

1.3.2 MOUNTING THE WJ-8718/488-2 COMPONENTS

1. Secure connector 488-J1 on the 488-W2 cable assembly (part number 380059-1) to the adapter plate and secure complete assembly to the rear panel.

2. Position the Type 794275-5-X Synthesizer Interface Assembly (488-A1) near slots 7 and 8 of the I/O Motherboard, A6. Locate the A7A1P1 cable from the Tuning Resolution Board and install the cable in 488-A1 board connector J4, identified by brown color code.

3. Locate the A9P1 cable from the BFO Switch and install the cable in 488-A1 board connector J2, identified by orange color code.

4. Locate the A8P1 cable from the Frequency Display Board and install the Cable in 488-A1 board connector J3, identified by red color code.

5. Dress the cables, position the Type 794275-X Synthesizer Interface Assembly (488-A1) board slot connectors 7 and 8, and seat securely.

6. Position the Type 796075 I/O Interface (488-A3) near slot 5 of the I/O Motherboard.

7. Locate cable assembly 488-W2, installed at the rear panel, and install connector 488-P4 in 488-A3 board connector J1, identified by white color code.

8. Dress the cables, position the 488-A3 board in slot connector 5 in the I/O Motherboard, and seat securely.

9. Position the Type 794308-1 IF Interface Assembly (488-A2) near slots 1 and 2 of the I/O Motherboard. Locate the A10P1 cable from the Lower Panel Control and install the cable in 488-A2 board connector J1, identified by yellow color code.

10. Dress the cables, position the 488-A2 board in I/O Motherboard slots 1 and 2, and seat securely.

11. Replace receiver top cover.

1.4 PREPARATION FOR OPERATION

Through the use of the WJ-8718/488-2 Option, up to 14 parallel-connected receivers can be controlled by one controller. Before remote operation, each receiver must be placed in the remote operating mode, and a valid receiver address must be established. Refer to **Figure 1-21**, Type 796075 I/O Interface Schematic Diagram, when reading the following information.

1.4.1 REMOTE OPERATING MODE

A receiver, designated as a listener, must be placed in the remote operating mode by depressing the front panel REMOTE button. If the receiver has not previously been commanded by a remote device, the first remote message received after power on will place the receiver in a remote state. The receiver can be addressed to talk regardless of the REMOTE switch position. The remote or local operating modes cannot be established by remote command, but can be monitored.

1.4.2 RECEIVER ADDRESS

Parallel data from the controller are applied to all receivers under control, but only the addressed receiver "recognizes" its address and accepts the data. The 5-bit address code is established by switch settings in the S1 switch assembly on the I/O Interface (488-A3). A closed switch denotes a logic 1 and an open switch denotes a logic 0. A valid receiver address can be any binary-coded number in the 0 through 30 range, as listed in **Table 1-2.**

Table 1-2. Receiver Address Codes

Receiver Address	S2-5	S2-4	S2-3	S2-2	S2-1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0

NOTE: 0 = open, 1 = closed

Table 1-2. Receiver Address Codes (Continued)

Receiver Address	S2-5	S2-4	S2-3	S2-2	S2-1
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
NOTE: 0 = open, 1 = closed					

The logic levels established by the switch settings are inverted at the outputs of tri-state buffer U4, and are loaded on the microprocessor bus lines when the processor addresses U4 and initiates a read operation. The processor writes the receiver address into a register internal to the microprocessor interface, 488-A3U1, and, until U1 is reset, the interface (488-A3U1) determines if the receiver address on incoming data is valid. The ability of U1 to perform this service ensures that the microprocessor is interrupted only when a valid data byte is waiting to be fetched or a byte is needed for transmission.

1.5 OPERATION

1.5.1 488-1975 INTERFACE BUS

The IEEE Standard 488-1975 Interface Bus is organized into three sets of signal lines: eight bidirectional data lines, three handshake lines, and five management control lines. The interface point between the bus and the receiver under control is a 24-pin Amphenol receptacle mounted in the rear panel of the receiver at the REMOTE INPUT. **Table 1-3** lists the 488 connector pin numbers with the respective interface signals and functions. **Figure 1-2** illustrates the bus structure.

1.5.1.1 Data Lines

A set of eight data input/output lines, DIO1 through DIO8, carry all address and parameter data from the receiver rear panel REMOTE INPUT through 488-A3J1 to non-inverting tranceivers U2A and U3A. A bit-parallel, byte-serial, negative logic form is used for the bidirectional transfer of data, received in one of two data modes dependent on the level of the ATN management line.

When the ATN line is low, data received are read as receiver address data which place the receiver in the listen, or talk, state. An unlisten data word can also be sent by the controller that unaddresses all previously addressed devices, allowing the devices to accept data when the DAV line is active (low) and the ATN line is high. Equipment address codes (**Table 1-2**) can be converted to standard ASCII (American National Standard Code for Information Interchange) characters. The address code is an 8-bit binary-coded word reflecting

Table 1-3. 488 Connector Pin Assignments

Pin Number	Signal	Description
1-4	DIO1-4	Data Input/Output Lines
13-16	DIO5-8	Data Input/Output Lines
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready For Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	SHIELD	Shield
17	REN	Remote Enable
18-23	GND	Ground
24	GND, LOGIC	Logic Ground

the levels established by the 488-A3S1 settings (**paragraph 1.4.2**) in the five least significant bits.

The format of data transfers on the DIO lines is discussed in greater detail in **paragraph 1.5.2.**

1.5.1.2 **Handshake Lines**

A three-wire handshake sequence facilitates the asynchronous, bidirectional transfer of each byte of data between up to 14 receivers and one controller. The data transfer rate adjusts to the slowest active device on the bus, allowing units with different input/output speeds to be interconnected. The handshake lines are DAV (Data Valid), NRFD (Not Ready For Data), and NDAC (Not Data Accepted). A brief description of each signal follows; refer to **Figure 1-3**, Handshake Sequence Timing Diagram to correlate the descriptions.

DAV - The level on the DAV line is established by the transmitting device to indicate the availability and validity of information on the DIO data lines. When DAV is high, data are considered invalid and when the signal level is low, data are considered valid.

NRFD - The logic level of the NRFD signal indicates the condition of readiness of device(s) connected to the bus. When one or all devices are not ready for data, the NRFD line is logic low (true); however, when all devices on the bus are ready to accept data the signal goes high (false: all are ready to accept data).

NDAC - The NDAC handshake signal indicates the condition of device(s) to accept data. This line is logic low (true: data has not been accepted) until data are accepted by the device(s) on the bus. When the last device has accepted the data, the NDAC signal goes high.

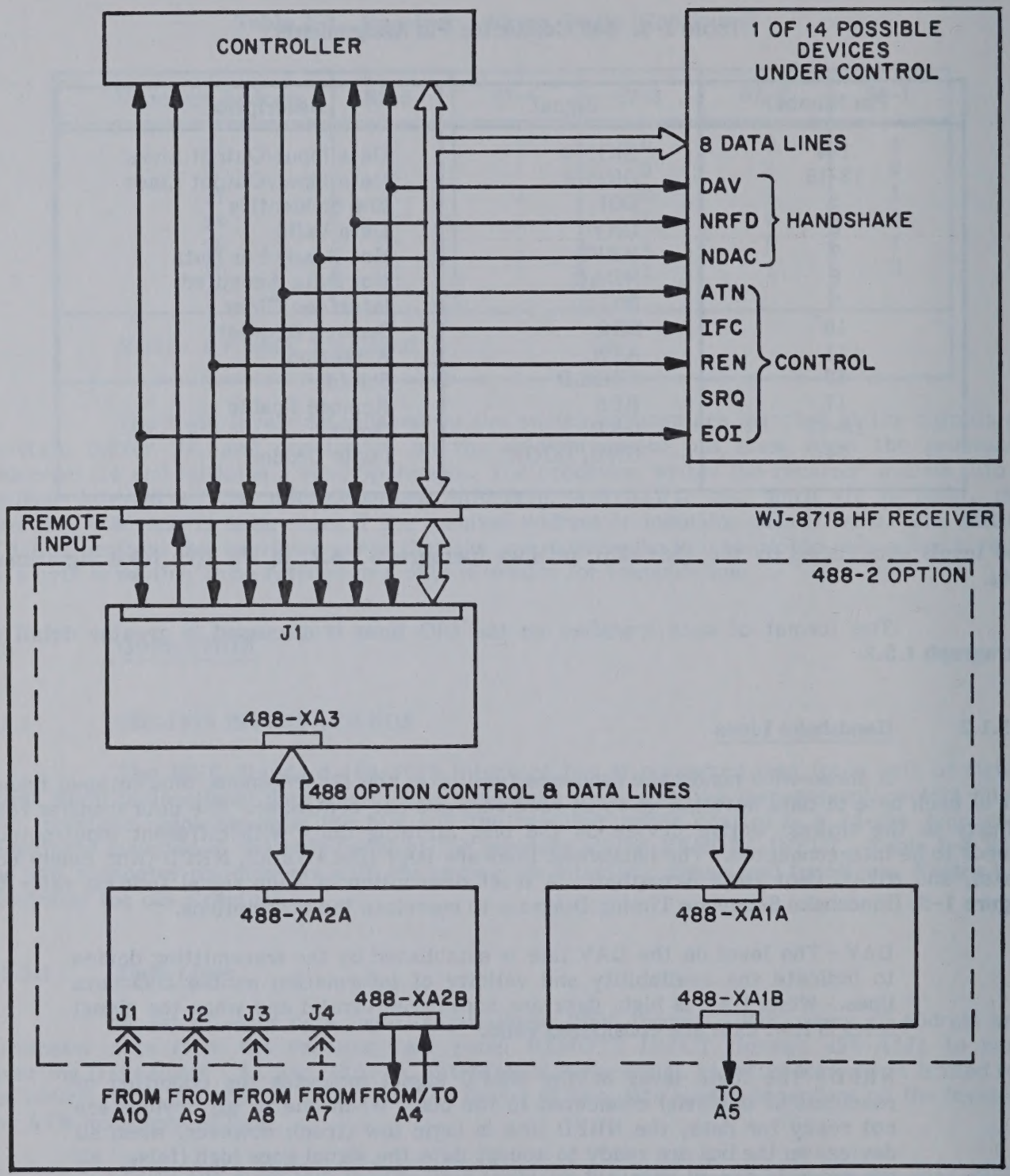

Figure 1-2. 488 Bus Structure and Interface Block Diagram

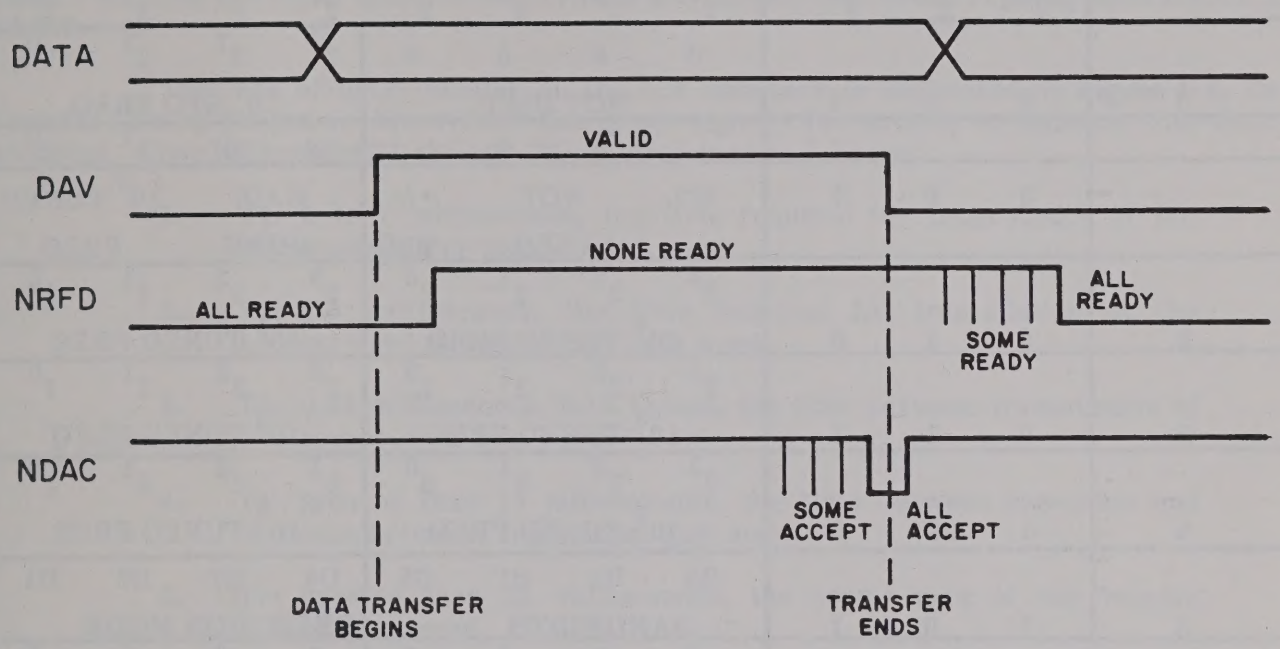

Figure 1-3. Handshake Sequence Timing Diagram

1.5.1.3 **Management Control Lines**

The management control signals manage an orderly flow of information across the bus. Three signals, ATN (Attention), REN (Remote Enable), and IFC (Interface Clear), are generated by the controller. The SRQ (Service Request) signal is generated by the device under control, and the EOI signal is generated by the transmitting device (controller or receiver).

The ATN line indicates how data on the DIO lines are to be interpreted; when ATN is low, data are read as receiver address data and, when high, as parameter data. The REN and IFC signals (active low) allow the controller to set and reset the interface system.

The SRQ signal indicates that the device under control requires attention. The EOI signal indicates the end of a multiple byte transfer sequence.

1.5.2 **PARAMETER DATA**

The full operating status of the receiver is contained in 57 bits of data, stored in eight 8-bit registers. The data associated with each register are listed in **Table 1-4.** Data

Table 1-4. Register Address Data

Register	Address			Data Word							
	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	0	0	0	2^3	2^2	2^1	2^0
				NOT USED				10^1 BFO FREQ			
1	0	0	1			0	0	G2	G1	2^1	2^0
				R/L	NOT USED		+/- BFO	GAIN MODE		10^7 TUNED FREQ	
2	0	1	0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
				10^6 TUNED FREQ				10^5 TUNED FREQ			
3	0	1	1	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
				10^4 TUNED FREQ				10^3 TUNED FREQ			
4	1	0	0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
				10^2 TUNED FREQ				10^1 TUNED FREQ			
5	1	0	1	B3	B2	B1	D5	D4	D3	D2	D1
				BANDWIDTH				DETECTION MODE			
6	1	1	0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	1^0
				10^3 BFO FREQ				10^2 BFO FREQ			
7	1	1	1	R/0	R/S	R/S	R/S	R/S	R/S	R/S	R/S
				*	MONITOR = SIGNAL STRENGTH(S)						
					COMMAND = RF GAIN (R)						

* Bit is unused in MONITOR Mode: must be 0
NOTE: BFO and TUNED frequencies in BCD (Hz)

Function Codes	
R/L: 1 = Remote, 0 = Local +/- BFO: 1 = -; 0 = +	GAIN MODE G2 G1 FAST AGC = 0 0 MANUAL = 0 1 SLOW AGC = 1 0
Bandwidth (in kHz) B3 B2 B1 16 = 0 0 0 6 = 0 0 1 3.2 = 0 1 0 1.0 = 0 1 1 0.3 = 1 0 0 OPT = 1 0 1	DET MODE D5 D4 D3 D2 D1 AM = 1 1 1 0 1 FM = 1 1 1 0 0 CW = 0 1 0 1 1 ISB† = 0 0 0 1 0 USB† = 0 0 0 0 1 LSB† = 0 0 0 0 0 †: SB selected, BFO Disabled
RF Gain (Command) Max (0) 0 0 0 0 0 0 0 0 Min (255) 1 1 1 1 1 1 1 1	Signal Strength (Monitor) No Signal (0) 0 0 0 0 0 0 0 Max (128) 1 1 1 1 1 1 1

transmission follows the required handshake signals. In the command mode, a register must be addressed before transmission of its data word; in monitor mode, the addressed receiver transmits an address header, followed by all bytes of parameter data, in the order listed in **Table 1-4.** The command and monitor formats are discussed in detail in **paragraphs 1.5.2.1** and **1.5.2.2.**

The rate of data transfer on the 488 interface is illustrated by **Figure 1-4,** Data Transfer Timing Diagram. The NDAC line is set high by the listener to indicate that data is accepted. Time references T1 through T5 are described as follows:

1. T1: 6 to 7 milliseconds, the time required for transmission of full status parameter data.

2. T2: 1.4 milliseconds, the time required for transmission of the address word up to the first data word.

3. T3: 0.24 milliseconds (4.1K bytes), the time between transmission of two consecutive data words.

4. T4: greater than 15 milliseconds, the time between reception and implementation of the manual gain word.

5. T5: greater than 30 milliseconds, the toggle rate of the remote manual gain word.

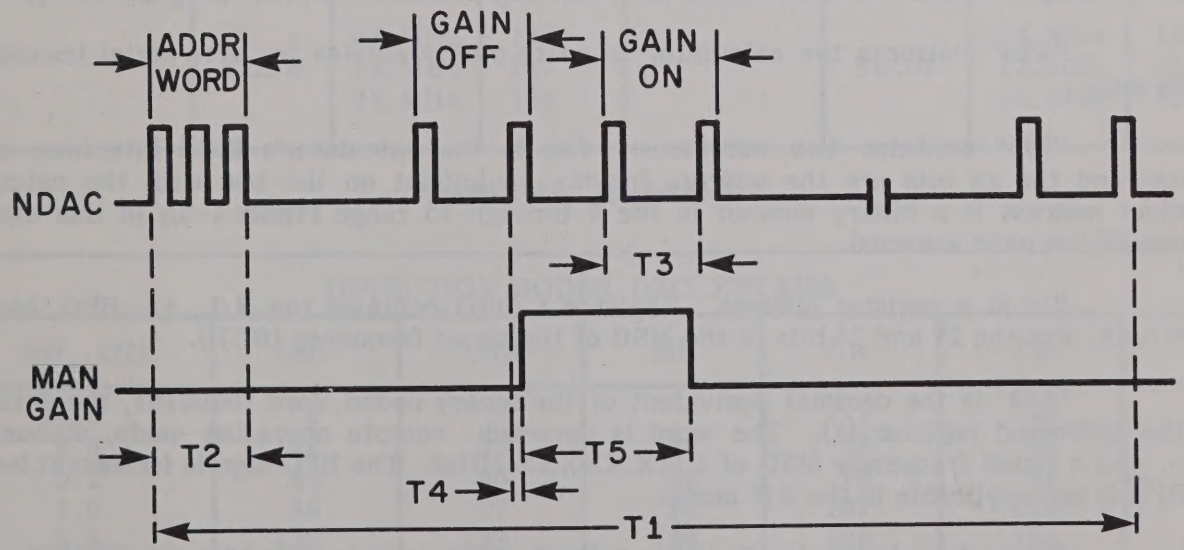

Figure 1-4. Data Transfer Timing Diagram

1.5.2.1 Command Data Format

In the command mode (receiver is a listener), three types of data words are transmitted by the controller: a receiver address word, a register address word, and a parameter data word corresponding to the register addressed (**Table 1-4**). To clarify the command data format, the following paragraph contains an example of programming technique using the Hewlett-Packard 9825A Calculator as the remote control device.

1.5.2.1.1 Remote Command Programming

The Hewlett-Packard 9825A is a typical remote control device compatible with the 488-1975 Interface Bus. The calculator converts decimal keyboard entries to a binary code which is applied to the receiver under control. **Table 1-5** lists the binary/decimal conversions for all receiver parameter data.

The command program is entered on the calculator keyboard as a serial string of decimal numbers, separated by commas. For example, assume that a receiver at address 06 is to be commanded to the following parameters:

Tuned frequency - 12.34567 MHz
Detection Mode - AM
Bandwidth - 1.0 kHz
BFO Frequency - Not applicable in AM
Gain Mode - Manual
RF Gain - 30

The entire program is entered: wtb, 706, 1, 133, 2, 35, 3, 69, 4, 103, 5, 125, 7, 30. Refer to **Tables 1-4** and **1-5** to correlate the following discussion of each program entry.

"wtb" instructs the calculator to write binary entries for byte-serial transmission on the bus.

"706" contains two addresses: 7xx is the calculator's IEEE interface module address and the xx bits are the address for the equipment on the bus with the calculator. Receiver address is a binary number in the 0 through 15 range **(Table 1-2);** in this example, address 06 has been assumed.

"1" is a register address. Register 1 (001) contains the R/L, +/- BFO, and gain mode data, plus the 2^0 and 2^1 bits of the MSD of the tuned frequency (BCD).

"133" is the decimal equivalent of the binary coded word 10000101, the data word for the addressed register (1). The word is decoded: remote operating mode, manual gain mode, and a tuned frequency MSD of 1 (1X.XXXXX MHz). The BFO sign is irrelevant because the BFO is not applicable in the AM mode.

"2" is the address for Register 2 (010) which contains the 10^5 and 10^6digits of the tuned frequency in BCD format.

"35" is the decimal equivalent of binary 00100011, the data word for the addressed register (2). The binary word represents BCD 23, the 10^5 and 10^6 digits of the tuned frequency (X2.3XXXX).

Table 1-5. Decimal Entries for Registers 0 Through 7

Table 1-5a. Registers 0, 2, 3, 4, and 6

BINARY	DEC.	BINARY	DEC.
0 → 9	= 0 → 9	30 → 39	= 80 → 89
10 → 19	= 16 → 25	60 → 69	= 96 → 105
20 → 29	= 32 → 41	70 → 79	= 112 → 121
30 → 39	= 48 → 57	80 → 89	= 128 → 137
40 → 49	= 64 → 73	90 → 99	= 144 → 153

Table 1-5b. Register 1

REM./LCL. +/- BFO	GAIN MODE	FREQ. 10^7	DEC. EQUIV.	REM./LCL. +/- BFO	GAIN MODE	FREQ 10^7	DEC. EQUIV.
REM. +BFO	FAST	0X.MHz	128	REM. -BFO	FAST	0X.MHz	144
		1X.MHz	129			1X.MHz	145
		2X.MHz	130			2X.MHz	146
	MAN	0X.MHz	132		MAN	0X.MHz	148
		1X.MHz	133			1X.MHz	149
		2X.MHz	134			2X.MHz	150
	SLOW	0X.MHz	136		SLOW	0X.MHz	152
		1X.MHz	137			1X.MHz	153
		2X.MHz	138			2X.MHz	154

Table 1-5c. Register 5

DETECTION MODES, DEC. ENTRIES						
BW, kHz	LSB	USB	ISB	CW	FM	AM
16.0	0	1	2	11	28	29
6.0	32	33	34	43	60	61
3.2	64	65	66	75	92	93
1.0	96	97	98	107	124	125
0.3	128	129	130	139	156	157
OPT.	160	161	162	171	188	189

"3" is the Register 3 (011) address. Register 3 contains the 10^3 and 10^4 digits of the tuned frequency.

"69" is the decimal equivalent of binary word 01000101, the data word for the addressed register (3). The word represents 45 in BCD or a tuned frequency of XX.X45XX.

"4" addresses Register 4 (100), the register for the 10^1 and 10^2 digits of the tuned frequency.

"103" is the decimal equivalent of binary 01100111, the data word for the addressed register (4). In BCD the word is 67; the tuned frequency is XX.XXX67 MHz.

"5" is the address for Register 5 (101) which contains bandwidth and detection mode data.

"125" is the decimal equivalent of binary 01111101, the addressed register (5) data word. The word contains the codes for 1.0 kHz bandwidth and AM detection mode.

"7" addresses Register 7 (111), the RF gain mode register in command mode.

"30" is the RF gain code and needs no conversion because the RF gain is specified as decimal entries from 0 through 255.

In summary, a remote command program consists of a string of decimal entries alternating between register addresses and data. The parameter data, preceded by the register address, can be entered in any order and parameters that are not to be changed are left out.

The MSB of the Register 1 data word is always high during remote control, indicating that the receiver is in remote operating mode. The bit is an indicator only; remote command cannot establish remote operating mode in the receiver. Remote operating mode is established by engaging the front panel TUNING DISABLE button.

1.5.2.1.2 Remote Monitor Programming

A monitor program begins with the transmission of a receiver address word which activates the I/O circuits in the addressed receiver, causing an interrupt signal to be generated to the microprocessor in the receiver control block. The microprocessor branches to an area of memory containing the current receiver parameter data. Receiver parameters are stored in sequential memory locations in the order listed in **Table 1-4.** The processor begins to transmit data at the location where a previous data transmission ended. The controller receives the transmitted data in binary-coded form and has no way of knowing which data are represented by the binary coded transmissions.

To synchronize the transmission of data, an address header precedes the parameter data words in memory. The address header is an 8-bit word containing the 5-bit receiver address in the lower-order bits; the 2^6 and 2^7 bits are high to uniquely identify the word as an address header (2^5 bit is irrelevant). After the address header has been transmitted and identified, the eight data words that follow will be the parameter data listed in **Table 1-4.**

The programmer uses a comparison technique to identify or "find" the address header. The first two bits of the binary-coded word are high (11XXXXXX); therefore, the decimal equivalent of the address header word is always greater than 192. The parameter data binary codes are such that the 2 MSDs are never high at the same time; thus, the decimal equivalent of a parameter data word will always be less than 192. By successively comparing the decimal equivalent of each transmitted word to 192, the address header can be isolated and the data words that follow can be identified.

Table 1-6 is a monitor program for the Hewlett-Packard 9825A Calculator. The first four program steps (0 through 3) establish a string of 15 spaces (A $[15]) for placement of parameter data, format the display readout, and load zeros into locations I and A.

Program steps 4, 5, and 6 establish two loops, or sets of program instructions, during which the address header and parameter data words will be identified and stored in consecutive locations. Step 4 instructs the calculator to read the binary coded data (rdb) received on the 488 interface (7XX) from the equipment at address 06 (X06) and to place the data word in register rI or r0 (→rI). In step 5, the program instruction is to examine registers A and rI and if A = 0 and rI is less than 192, return to, and repeat, step 4. This procedure (loop) will repeat until the decimal equivalent of the binary coded data word, stored in rI, is greater than 192 (the only data word greater than 192 is the address header word); at this point, the program jumps out of the loop to step 6.

In step 6, the rI is incremented and A is loaded with a 1; if rI is less than 9 (rI is now 1), the program returns to step 4. The received data word is read and placed in rI (now in r1, one location away from the address header word in location r0) and the program advances to step 6. Again, rI is incremented (I + 1 = I or 1 + 1 = 2 = I) and the loop repeats until I = 9 when the program jumps out of the loop to step 7. The contents of r0 are reduced by 192; at this point r0 contains the address and r1 through 8 contain the receiver parameter data words in the order listed in **Table 1-4.**

Program steps 8 through 22 are a combination of binary AND, shift, and comparisons operations which isolate the information in the parameter data words. For example, in step 14, the contents of r6 (in **Table 1-4,** the register 5 data) are ANDed with 31 (00011111), extracting the lower 5 bits of detection mode data, which are placed in Q. In step 15 the r6 contents are shifted right five places; the three LSBs of the data word now contain the bandwidth code and all other bits are zeros. This data word is placed in R.

Steps 23 through 42 of the program place the data (derived in steps 8 through 22) in the string reserved in step 0. For example, in step 24, if Q = 29, the selected detection mode is AM (**Table 1-5**); A is placed in the 3rd place and M is placed in the 4th place in the string ("AM"→$[3, 4]).

If the receiver under control is equipped with the 10 Hz BFO Option, Register 0 (r1) will contain the BCD 10^1 frequency digit. In program step 43, the contents of r1 are compared to 9; if the register is used the decimal equivalent of the binary-coded data word will be less than 9 and the contents of r1 will remain intact. If the register is unused, all bits will be high, or greater than 9, and a 0 will be loaded into r1 (if r1>9; 0→r1).

In the remaining steps of the program, the calculator is instructed to display the receiver address and the parameters in the following order: R/L status, detection mode, bandwidth, gain mode, BFO sign, three digits of BFO frequency, signal strength, and seven digits of RF tuned frequency.

Table 1-6. Monitor Program

```
0: dim A$[15];fxd 0
1: prt "READ TEST"
2: fmt f1.0,".",2f1.0," ",f3.0," ",2f1.0,".",5f1.0
3: 0→I;0→A
4: "loop":rdb(706)→rI
5: if A=0 and rI<192;gto "loop"
6: I+1→I;1→A;if I<9;gto "loop"
7: r0-192→r0
8: band(r3,15)→J
9: shf(r3,4)→I
10: band(r4,15)→L
11: shf(r4,4)→K
12: band(r5,15)→P
13: shf(r5,4)→M
14: band(r6,31)→Q
15: shf(r6,5)→R
16: band(r7,15)→O
17: shf(r7,4)→N
18: band(r2,3)→H
19: if r2>=128;1→V;gto +2
20: 0→V
21: band(r2,16)→U
22: band(r2,12)→T
23: " "→A$[1,15]
24: if Q=29;"AM"→A$[3,4]
25: if Q=28;"FM"→A$[3,4]
26: if Q=11;"CW"→A$[3,4]
27: if Q=2;"ISB"→A$[3,5]
28: if Q=1;"USB"→A$[3,5]
29: if Q=0;"LSB"→A$[3,5]
30: if R=0;"16KHz"→A$[7,11]
31: if R=1;"6KHz"→A$[7,10]
32: if R=2;"3.2KHz"→A$[6,11]
33: if R=3;"1KHz"→A$[7,10]
34: if R=4;".3KHz"→A$[7,11]
35: if R=5;"opt"→A$[8,10]
36: if T=0;"F"→A$[13,13]
37: if T=4;"M"→A$[13,13]
38: if T=8;"S"→A$[13,13]
39: if U=0;"+"→A$[15,15]
40: if U=16;"-"→A$[15,15]
41: if V=0;"L"→A$[1,1]
42: if V=1;"R"→A$[1,1]
43: if r1>9;0→r1
44: wrt 0,A$,N,O,r1,r8,H,I,J,K,L,M,P
45: if X=0;prt "RECEIVER ADDRESS",r0;spc 2
46: 1→X;gto 3
*29368
```

1.6 FUNCTIONAL DESCRIPTION

The WJ-8718/488-2 Option consists of three circuit boards, one which contains an Intel 8085A Microprocessor with memory, read-only, write-only, and input/output devices to support the microprocessor. **Figure 1-5** is the WJ-8718/488-2 Block Diagram.

The functional descriptions in **paragraphs 1.6.1** through **1.6.4.5** concern the microprocessor and the functional areas directly related to the microprocessor. **Paragraphs 1.6.5** through **1.6.7** contain functional descriptions of each board in the option and are followed by detailed circuit descriptions in **paragraphs 1.7.1** through **1.7.3.**

1.6.1 INPUT/OUTPUT PORT

The microprocessor requires an input/output port to communicate with the remote control equipment via the 488-1975 Interface Bus. The I/O port is an integrated circuit on the I/O Interface, 488-A3. The circuit is a microprocessor-controlled chip designed to implement all of the 488 bus functions (except for the controller). Capabilities of the I/O device include data transfer, handshake protocol, talker/listener addressing procedures, service request, and serial and parallel polling schemes.

1.6.2 MEMORY DEVICES

Memory provides locations to store instructions and data for the microprocessor. The processor deals with 8-bit binary fields and the memory associated with the processor is organized to store eight bits in each location. Data and instructions are stored in memory as 8-bit binary numbers or as numbers that are integral (even) multiples of eight bits: 16 bits, 24 bits, and so on. This characteristic 8-bit field is referred to as a byte. Each byte is stored in a memory location that is numbered to distinguish it from all other locations. The number which identifies a memory location is called its address.

A group of logically related instruction words, or program, is stored in sequential memory locations. The microprocessor reads each instruction in memory in a logically determined sequence and uses it to initiate processing actions. The instruction program is stored in an EPROM integrated circuit on the Synthesizer Interface Board, 488-A1.

An addressable area of memory is required to store receiver parameter data so that the data can be accessed for transmission when a remote control equipment request is received, or accessed to be updated as locally or remotely selected receiver parameters are changed. Memory for this purpose is provided by RAM integrated circuits on the Synthesizer Interface Board, 488-A1. The RAM also provides an area of memory which the microprocessor uses as a "scratch pad", to temporarily store data being processed. Another area of RAM is used as a stack, described in **paragraph 1.6.4.1.1.**

1.6.3 READ-ONLY/WRITE-ONLY DEVICES

Flip-flop and buffer integrated circuits on the 488-A1, A2, and A3 boards serve as addressable read-only and write-only devices. Read-only devices allow the microprocessor to monitor the status of the receiver's front panel controls; write-only devices allow the microprocessor to update receiver parameters.

1.6.4 MICROPROCESSOR

The microprocessor, located on 488-A2, unifies the system by controlling the functions of memory, input/output, read-only, and write-only devices. The processor must be able to access, decode, and execute the binary coded instructions in the program. During the execution of the program, the microprocessor must be able to reference memory, if necessary, and must be able to recognize and respond to the interrupt signal from the I/O port. The microprocessor meets its obligations by utilizing internal circuits as illustrated by **Figure 1-6**, the Intel 8085A Microprocessor Block Diagram. A brief description of the operation of key functional areas within the microprocessor follows.

1.6.4.1 Registers

Registers are temporary storage units within the microprocessor. Some registers, such as the program counter, flag register, stack pointer, and instruction register have dedicated uses. The accumulator and all other general purpose registers are used for storage of intermediate data during the execution of instructions. The accumulator is also used during arithmetic operations.

1.6.4.1.1 Program Counter and Stack Pointer

The instructions that make up the program are stored in EPROM (Erasable Programmable Read-Only Memory) on the 488-A1 board. The microprocessor references the contents of the memory in order to determine what action is appropriate. This means that the processor must know which location contains the next instruction. The processor maintains a register which contains the address of the next program instruction. This register is the program counter. Because the microprocessor updates the program counter each time it fetches an instruction, the program counter is always pointing to the next instruction.

The program is stored in EPROM in numerically adjacent addresses (beginning at location zero). The lower order addresses contain the first instructions to be executed and the higher order addresses contain the later instructions. During the course of the instructions, the program may call, or transfer control to, a subroutine. A subroutine is a program within a program; often, it is a general purpose set of instructions which must be executed repeatedly during the program. Memory space is conserved by storing the instructions in an area apart from the main program and directing the processor to this area as necessary. The subroutine instructions are also stored in numerically adjacent addresses in EPROM. When a subroutine is called, the processor is instructed to jump to the lowest subroutine address. After the subroutine is finished, the processor must resume execution of the main program; therefore, the processor must remember the contents of the program counter at the time the call occurs.

The microprocessor has a special way of handling subroutines in order to ensure an orderly return to the main program. When the processor receives a call instruction, it increments the program counter and stores the counter's contents in a reserved area in RAM on the 488-A1 board. This memory area is called a stack. The stack saves the address of the instruction to be executed after the subroutine is completed. Next, the processor loads the subroutine address in its program counter, ensuring that the next instruction fetched will be the first step of the subroutine.

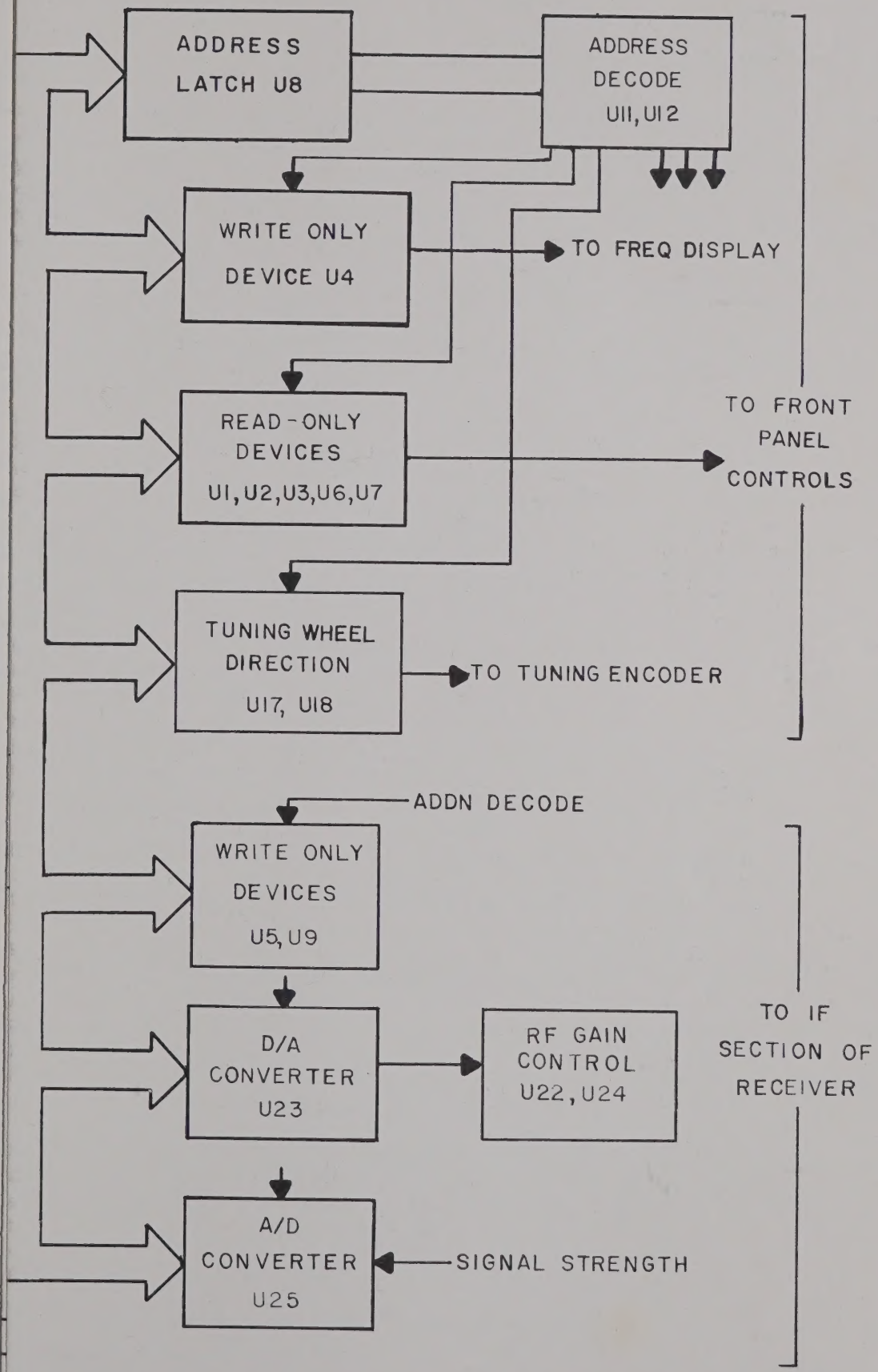

Figure 1-5. WJ-8718/488-2 Option Block Diagram

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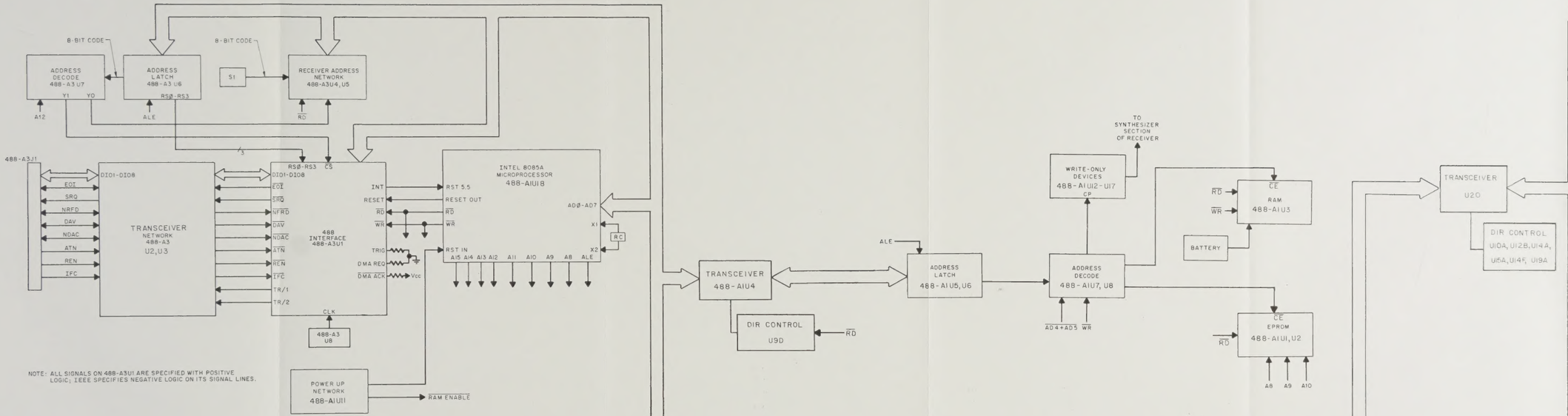

Figure 1-5. WJ-8718/488-2 Option Block Diagram

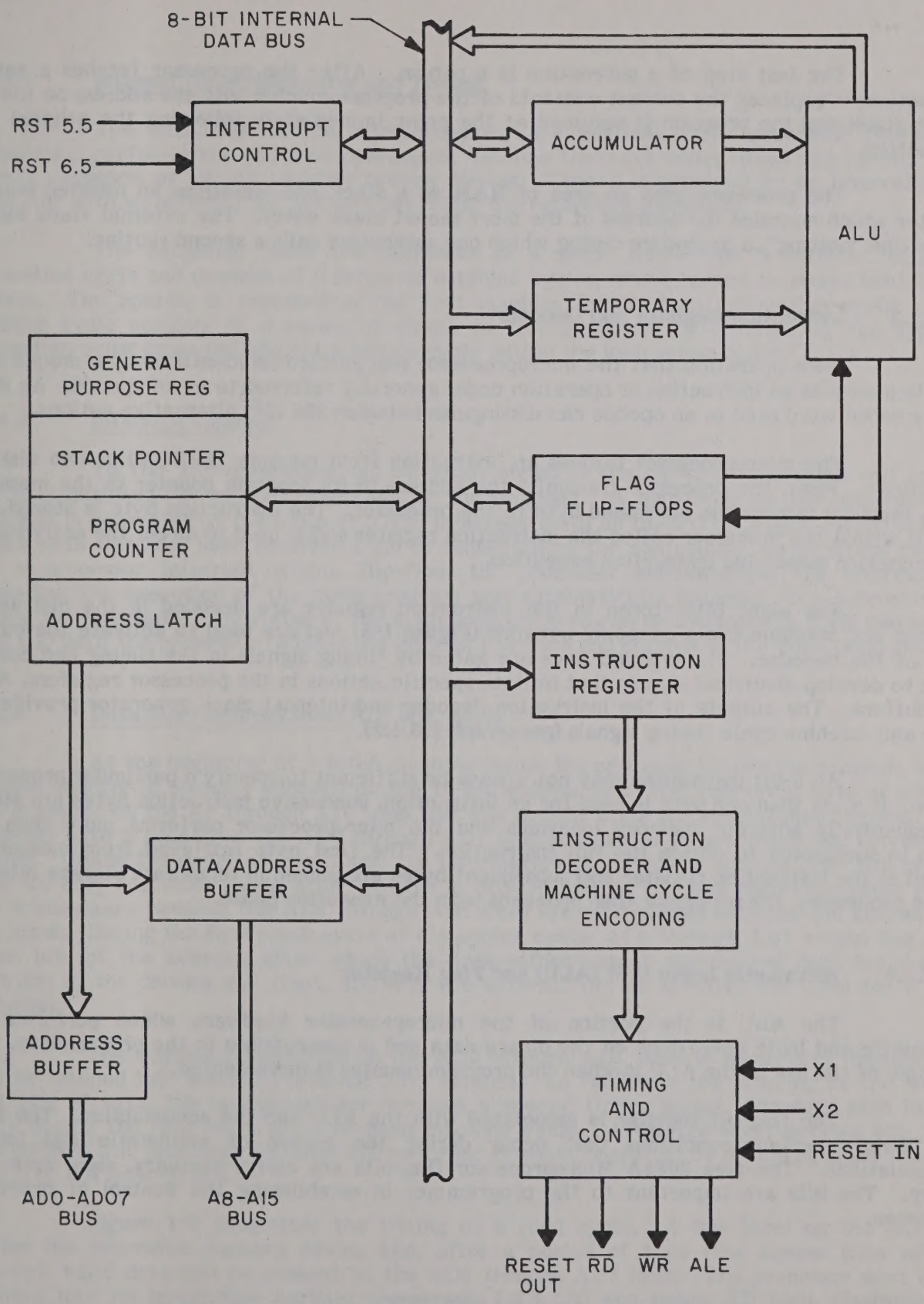

Figure 1-6. Intel 8085A Microprocessor Block Diagram

The last step of a subroutine is a return. After the processor fetches a return instruction, it replaces the current contents of the program counter with the address on the top of the stack and the program is resumed at the point immediately following the original call instruction.

The processor uses an area of RAM as a stack and maintains an internal pointer register which contains the address of the most recent stack entry. The external stack allows subroutine "nesting", a procedure during which one subroutine calls a second routine.

1.6.4.1.2 **Instruction Register and Decoder**

Each operation that the microprocessor can perform is identified by a unique byte of data known as an instruction or operation code, generally referred to as an opcode. An 8-bit binary coded word used as an opcode can distinguish between 256 (2^8) alternative actions.

The microprocessor fetches an instruction from memory (EPROM) in two distinct operations. First, the processor transmits the address in its program counter to the memory. Next, memory returns the addressed byte to the processor. The instruction byte is stored in a circuit within the processor called the instruction register and is used to direct the activities of the processor during the instruction execution.

The eight bits stored in the instruction register are decoded in the instruction decoder and machine cycle encoding network (**Figure 1-5**) and are used to activate the output lines of the decoder. The enabled lines are gated by timing signals in the timing and control block to develop electrical signals that initiate specific actions in the processor registers, ALU, and buffers. The outputs of the instruction decoder and internal clock generator provide the state and machine cycle timing signals (**paragraph 1.6.4.2**).

An 8-bit instruction may not always be sufficient to specify a particular processing action. If more than one byte is used for an instruction, successive instruction bytes are stored in sequentially adjacent memory locations and the microprocessor performs more than one fetch in succession to obtain the full instruction. The first byte retrieved from memory is placed in the instruction register and subsequent bytes are placed in temporary storage internal to the processor; the processor then proceeds with the execution phase.

1.6.4.1.3 **Arithmetic Logic Unit (ALU) and Flag Register**

The ALU is the portion of the microprocessor hardware which performs the arithmetic and logic operations on the binary data and is inaccessible to the programmer. (An example of the use of the ALU is when the program counter is incremented.)

The flag-bit register is associated with the ALU and the accumulator. The flag-bits specify certain conditions that occur during the course of arithmetic and logical manipulations. The five 8085A Microprocessor flag-bits are carry, auxiliary, sign, zero, and parity. The bits are important to the programmer in establishing the control of processor operation.

1.6.4.2 Internal Clock Generator and Timing

The activities of the microprocessor are cyclical. The processor fetches an instruction, performs the required operations, fetches the next instruction, and so on. This orderly sequence of events requires precise timing. Timing is provided by an internal clock generator with an external RC network providing the reference frequency.

The combined fetch and execution of a single instruction is referred to as an instruction cycle and consists of a series of machine cycles, whose nature is determined by the opcode. The opcode is accessed in the first machine cycle of an instruction cycle. Each machine cycle consists of a series of clock, or timing, cycles determined by the type of instruction being executed and the machine cycle within the instruction cycle.

1.6.4.3 Interrupt Control

To the microprocessor, an interrupt signal is similar to a subroutine call except that it is initiated externally rather than by the program. A high level on the interrupt line (RST 5.5) is generated by the I/O port (GPIB Interface card) on the I/O Interface Board (488-A3) when a data word has been received from or requested by the controller. An interrupt request sets a processor interrupt enable flip-flop; the processor acknowledges the interrupt by suspending the execution of the main program and automatically branches to a subroutine to service the interrupt. The status of the main program is stored on the stack in RAM (**paragraph 1.6.4.1.1**) until the processor finishes the interrupt service and returns to the main program.

1.6.4.4 Data Bus Control Lines ($\overline{RD}$, $\overline{WR}$, ALE)

At the beginning of a fetch machine cycle, the processor places the contents of the program counter (a memory address) on the 16-bit address bus. The high-order byte of address data is placed on the A8 through A16 lines and will remain there for several clock cycles. The low-order byte is placed on the AD0 through AD7 lines and the microprocessor line drivers are enabled. Unlike the upper address lines, the information on the lower address lines will remain there for only one clock cycle after which the drivers will go to their high-impedance state. This is necessary because the AD0 through AD7 lines are multiplexed between the address and data buses. During the first clock cycle of a machine cycle, AD0 through AD7 output the eight lowest bits of the address, after which the lines either output the desired data for a write operation or the drivers will float, allowing the external device to drive the lines for a read operation.

The address information on the AD0 through AD7 lines is transitory, therefore, it must be latched into selected external 8-bit latches. To facilitate the latching of the lowest eight bits of data, the microprocessor provides a special timing signal, Address Latch Enable (ALE), during the first clock state of each machine cycle. After the eight address bits have been latched, the processor initiates either a read or write operation by providing a low level on the $\overline{RD}$ or $\overline{WR}$ control line.

Figure 1-7 illustrates the timing of a read cycle. A low level on the $\overline{RD}$ line enables the addressed memory device and, after a period of time (the access time of the memory), valid data will be present on the AD0 through AD7 lines. The processor next loads the data into its instruction register (**paragraph 1.6.4.1.2**) and raises $\overline{RD}$ high, disabling the addressed memory device.

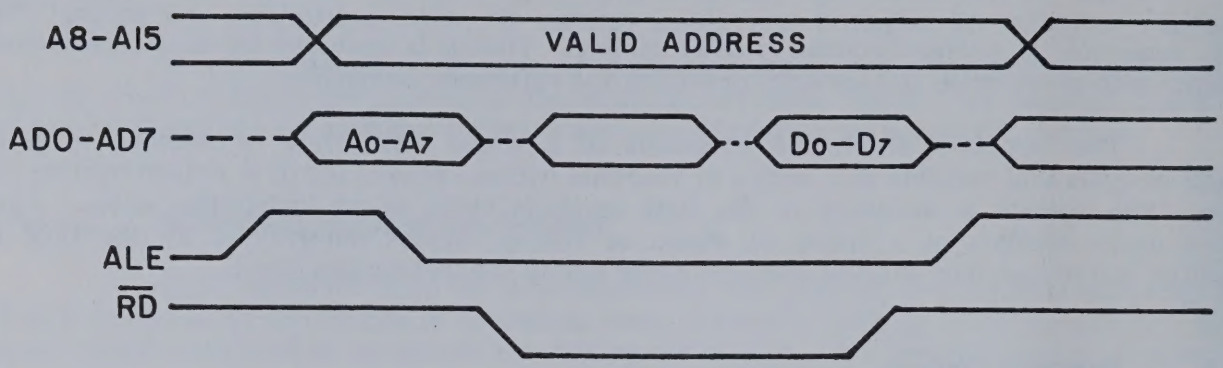

Figure 1-7. $\overline{RD}$ Timing Diagram

After ALE drops, a low level on the $\overline{WR}$ line causes data to be placed on the AD0 through AD7 lines by the processor. The data are loaded into the addressed memory when $\overline{WR}$ goes high. **Figure 1-8** illustrates a write timing pulse.

The A8 through A15 data lines are used to identify the MSBs of a memory or I/O location for a data transfer cycle. Selected bits provide enabling pulses to address decode circuits which, in turn, provide enabling pulses to read-only and write-only registers on the 488-A1, A2, and A3 boards. See the detailed circuit descriptions, **paragraphs 1.7.1** through **1.7.3** for more details.

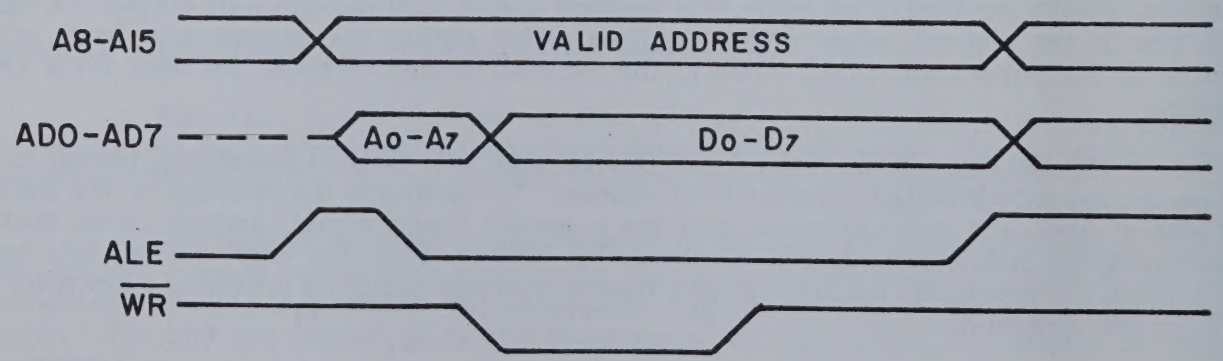

Figure 1-8. $\overline{WR}$ Timing Diagram

1.6.4.5 Reset In/Reset Out

The microprocessor is reset when the RESET $\overline{IN}$ line is low and commences execution of its program when the line goes high. The RESET OUT line goes high to reset the 488-A3 communications interface circuit (I/O port).

1.6.5 I/O INTERFACE BOARD

The primary function of the I/O Interface is to handle communications between the remote control equipment and the receiver's microprocessor control block. A bit-parallel, byte-serial negative logic form is used in the bidirectional transfer of data. Handshake and management control signals allow an orderly data flow. The I/O port signals the microprocessor when data are received and ready to be fetched or when data are needed for transmission.

A switch assembly on the I/O Interface is used to establish receiver address (**paragraph 1.4.2**).

1.6.6 IF INTERFACE BOARD

The IF Interface Board (488-A2) replaces the Front Panel Interconnect Board (A2) in the WJ-8718 HF Receiver. The IF Interface Board contains D/A and A/D converters (for RF gain and signal strength voltages), and write-only latches for driving the IF sections of the receiver.

1.6.7 SYNTHESIZER INTERFACE BOARD

The microprocessor, which is the central control unit of the addressed receiver, is mounted on this board. The microprocessor is reset when the receiver is energized. Immediately, the processor initiates its program at location zero in memory. Following a pre-programmed sequence, the microprocessor proceeds to fetch instructions from sequential memory locations and perform the operations necessary to carry out the instructions. See **paragraphs 1.6.4** through **1.6.4.5** for a functional description of processor activities.

A pre-programmed EPROM integrated circuit on the Synthesizer Board contains 8-bit memory locations from 0000 to 0FFF. The instructions for the microprocessor are stored in the EPROM and are read sequentially by the microprocessor.

The microprocessor begins its program by fetching the contents of location 0000 in the EPROM. If the complete instruction is stored in more than one location, the microprocessor stores the contents of 0000 in its own internal registers and returns to the EPROM to read location 0001. The microprocessor continues to fetch and store instructions until it has enough information. A program counter internal to the microprocessor is constantly updated with the addressed memory location. When an instruction is complete, the microprocessor executes the instruction, and returns to the EPROM to fetch the next instruction in the sequence. The procedure continues until the microprocessor is instructed to return to the beginning of the program.

During the course of the program, the microprocessor will read into or write from an addressed peripheral device. During a write instruction, the microprocessor may address RAM or a write-only peripheral device. Six write-only registers on the Synthesizer Interface

Board shift received RF and BFO data to the receiver's display section and to the RF and BFO synthesizers. During read programs, the microprocessor monitors the status of front panel controls. The monitored data are transmitted to the remote control equipment via the I/O board. RAM integrated circuits on the Synthesizer Interface Board are used to store transitory data.

1.7 DETAILED CIRCUIT DESCRIPTION

Refer to **Figures 1-19** through **1-22** to correlate the following circuit descriptions, written in order of the reference designations.

1.7.1 TYPE 794275-X SYNTHESIZER INTERFACE AND MEMORY BOARD (488-A1)

The Synthesizer Interface Board replaces the Manual Tuning Up/Down Counter (A6A1) in the WJ-8718 HF Receiver. The board contains the Intel 8085A Microprocessor, which is the control for the MFP Option. Random Access Memory (RAM) provides temporary storage, and Erasable Programmable Read-Only Memory (EPROM) contains the microprocessor's instruction program. The board interfaces the microprocessor data bus with the BFO and LO Synthesizers through data latches. **Figure 1-9** is a simplified block diagram of the 488-A1 board and **Figure 1-19** is the schematic diagram.

1.7.1.1 Microprocessor (U18)

The Intel 8085A Microprocessor is an 8-bit general purpose microprocessor that requires a single +5 V supply. The microprocessor contains eight addressable 8-bit general purpose registers and two 16-bit non-addressable registers which make up the CPU.

A multiplexed data bus allows the microprocessor to communicate with external devices. The execution of the microprocessor program consists of a series of machine cycles. Each machine cycle contains a series of clock cycles. During the first clock cycle of a machine cycle, an external device address is placed on the data bus. The address is divided between the higher-order 8-bit address (A8 through A15) and the lower-order 8-bit address/data bus (AD0 through AD7). The eight lower-order address bits are latched into external devices by the Address Latch Enable (ALE) signal. During the remaining portion of the machine cycle the bus is used for data.

The microprocessor provides $\overline{RD}$, $\overline{WR}$, and ALE outputs for bus control; and RST 5.5, RST 6.5, and RST 7.5 for interrupts. RST 7.5 is used for timing events and is driven by an RC oscillator circuit U11B and U11C. RST 5.5 and RST 6.5 are only used when an optional remote I/O is installed.

The microprocessor is driven by oscillator circuit U11E and U11D at a frequency of approximately 2 MHz; this is internally divided by 2 to give the bus an operating speed of 1 MHz.

1.7.1.2 Power Up/Down Circuit (U11)

The Power Up/Down Detect circuit drives the $\overline{RESET\ IN}$ input to the Intel 8085A Microprocessor. When this input goes low all operations stop and all bus outputs become a high

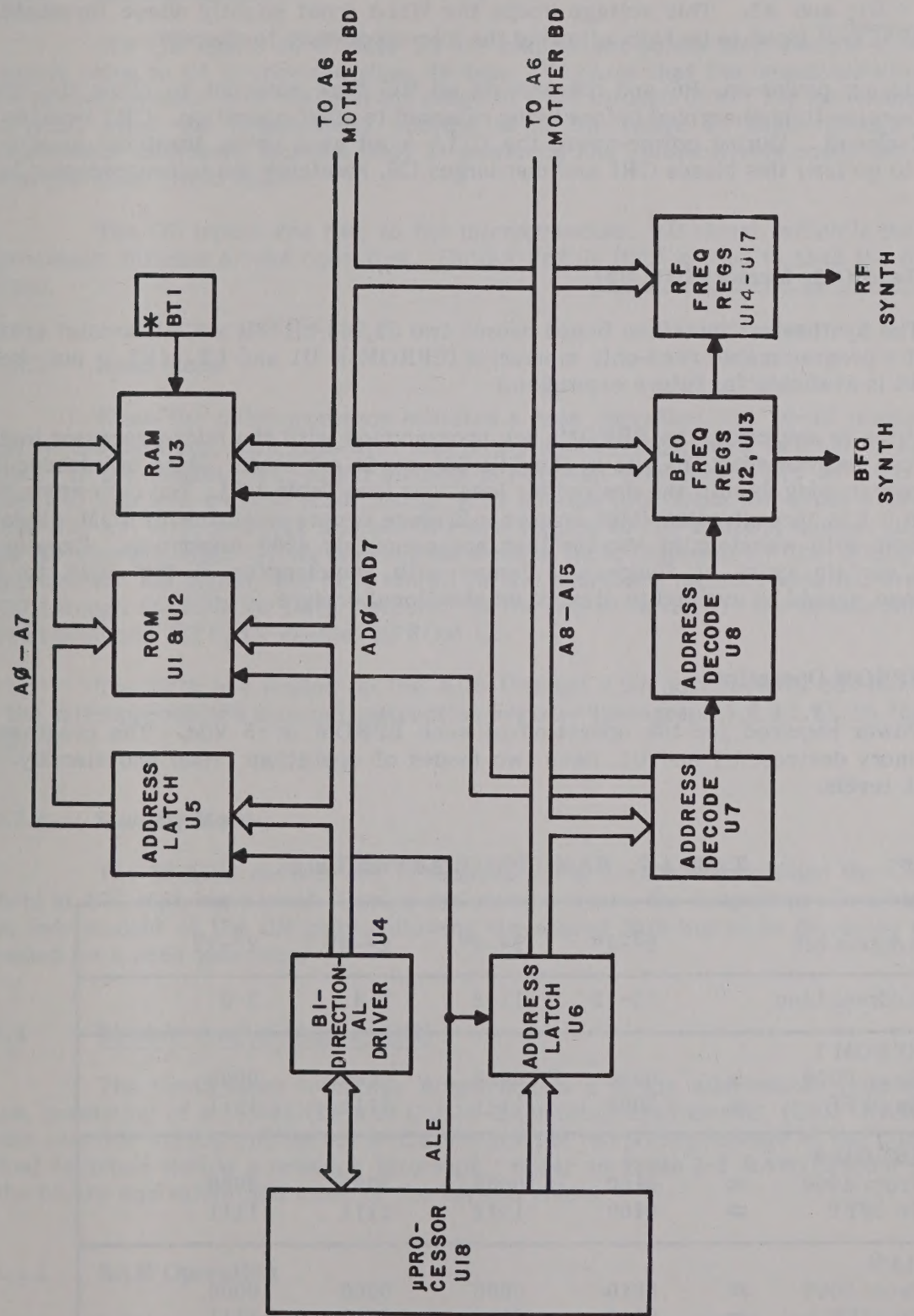

Figure 1-9. Synthesizer Interface and Memory Board, Simplified Block Diagram

impedance state. The input to the circuit is unregulated 10 V, dropped to approximately 1.5 V by VR1, R2, CR1, and R3. This voltage keeps the U11A input slightly above threshold and enables the $\overline{\text{RESET IN}}$ input to be high, allowing the microprocessor to operate.

During power-on, R6 and C9 provide an RC time constant to allow the microprocessor to become fully energized before being released to start operation. CR2 isolates U11 from the RC circuit. During power-down, the U11A input goes below threshold causing the U11F output to go low; this biases CR1 and discharges C9, resetting the microprocessor in the process.

1.7.1.3 Read-Only Memory (U1, U2)

The Synthesizer Interface Board houses two 32,768-bit (8K x 8) ultraviolet erasable and electrically programmable read-only memories (EPROMs), U1 and U2. (U2 is not used in this design, but is available for future expansion.)

Prior to shipment, the EPROMs are programmed with the microprocessor instruction set. Before programming, all bits in the EPROM are in a 1 state. Data is introduced by selectively programming 0s into the desired bit locations (see **Table 1-7**). The only way a 0 can be changed to a 1 is through ultraviolet erasure. Erasure occurs when the EPROM window is exposed to light with wavelengths shorter than approximately 4000 Angstroms. Exposure to sunlight, and certain types of fluorescent lamps with wavelengths in the 3000 to 4000 Angstroms range, should be avoided to prevent unintentional erasure.

1.7.1.3.1 EPROM Operation

Power required for the operation of each EPROM is +5 Vdc. The programmed read-only memory devices, U1 and U2, have two modes of operation: read and standby. All inputs are TTL levels.

Table 1-7. RAM/EPROM Address Data

Address bit		2^3-2^0	2^3-2^0	2^3-2^0	2^3-2^0
Address Line		15-12	11-8	7-4	3-0
EPROM 1					
From 0000	=	0000	0000	0000	0000
To 0FFF	=	0000	1111	1111	1111
EPROM 2					
From 4000	=	0100	0000	0000	0000
To 4FFF	=	0100	1111	1111	1111
RAM					
From 2000	=	0010	0000	0000	0000
To 27FF	=	0010	0111	1111	1111

1.7.1.3.2 Control Inputs

The $\overline{CE}$ inputs to U1 and U2 are chip-select pulses from decode circuit U7. The low enable pulse to U1 is provided when decoder U7 senses that the hexadecimal-coded address on the microprocessor data bus is in the range of 0000 through 0FFF; the low enable pulse to U2 is provided when the hexadecimal address is in the range of 4000 through 4FFF. The microprocessor addresses location 0000 at power-up and consecutively reads and executes the instructions stored in EPROM.

The OE inputs are tied to the microprocessor $\overline{RD}$ signal, which is pulled low when the processor initiates a read operation. Output Enable (OE) is used to take the outputs out of tri-state.

1.7.1.3.3 Read Mode

When the microprocessor initiates a read operation, the 16-bit memory address is placed on the data bus, ALE goes low, and if the memory addressed is RAM or EPROM, U7 is enabled. If the hexadecimal-coded address is between 0000 and 0FFF, U7 pulls the U1 Chip Enable ($\overline{CE}$) line low, and the AD0 through AD7 address bits (from low-order address latch U5) and the A8, A9, A10, and A11 address bits are applied to the EPROM device through Address Inputs A0 through A11. After an address access time, followed by the falling edge of the microprocessor $\overline{RD}$ signal, the data stored in the addressed memory location are available at the O0 through O7 EPROM Data Outputs. In the same manner, if the hexadecimal address is between 4000 and 4FFF, U7 enables EPROM U2.

The data are loaded on the AD0 through AD7 address/data bus lines and latched into the microprocessor's internal instruction register (**paragraph 1.6.4.1.2**), on the rising edge of $\overline{RD}$.

1.7.1.3.4 Standby Mode

The EPROM devices are in reduced power standby mode when the $\overline{CE}$ enable lines are held at TTL high logic level. During the standby mode, the outputs are in a high impedance state, independent of the OE input, allowing the shared data bus to be driven by other devices addressed for a read operation.

1.7.1.4 Random Access Memory (U3)

The Synthesizer Interface Board houses a single addressable read/write memory device, consisting of a 16,384 (2K x 8) CMOS RAM integrated circuit, (U3). RAM stores data, current receiver status, and serves as a stack for the temporary storage of the microprocessor's internal registers during a program interrupt. Refer to **Table 1-7** RAM/EPROM Address Data for the binary equivalent addresses of the various chips.

1.7.1.4.1 RAM Operation

Power required for the operation of RAM U3 is +5 Vdc. The modes of operation consist of read, write, high-Z, and low power.

1.7.1.4.2 Control Input

The $\overline{CE}$ input from decoder U7 goes low when the hexadecimal address on the microprocessor data bus is in the range of 2000 through 27FF.

The read and write inputs are connected to the microprocessor $\overline{RD}$ and $\overline{WR}$ bus control signals and are active (low) for their respective bus cycles.

1.7.1.4.3 Read Mode

When the decoded address is in the 2000 to 27FF range and the microprocessor initiates a read operation, all bus cycles are identical to the read operation previously described for EPROM (see **paragraph 1.7.1.3.3**).

1.7.1.4.4 Write Mode

When the decoded address is in the range of 2000 to 27FF and the microprocessor initiates a write operation, decoder U7 output Y2 becomes active (low) and enables U3 address inputs A0-A10. During the data portion of the bus cycle, $\overline{WR}$ line becomes active (low) and a rising edge of $\overline{WR}$ causes data to be written into the internal address selected by A0-A10.

1.7.1.4.5 High-Z Mode

Any microprocessor bus cycle that does not enable U1, U2, or U3 leaves all outputs in a high-Z (high impedance) state. This disables the devices from having any effect on the bus.

1.7.1.4.6 Low Power Mode

RAM U3, being CMOS, can be kept powered on to maintain all data stored in the memory by holding Vcc/Vdd and $\overline{CE}$ to a 2 V level. Buffer U10D provides isolation for $\overline{CE}$ with power off; its open collector output is pulled up by R14.

1.7.1.4.7 Battery Backup

An inherent quality of RAM is that it is volatile, meaning that data is not retained when power is removed. To prevent the loss of data, a battery (BT1) is used to power the RAMs when power is down.

Transistor Q1, forward biased by Vcc when power is on, charges the 2.4 V battery through R4 and R5. When power is down, Vcc drops to zero and the transistor becomes reverse biased, allowing current to flow only to the RAM circuits connected to Vdd.

1.7.1.5 Bidirectional Bus Transceiver (U4)

Transceiver (U4) is made up of 16 high-speed CMOS buffer drivers, only eight of which are enabled at the same time. The direction of the data (or which eight buffers are

enabled) is controlled by the DIR input and is connected to the $\overline{RD}$ line of the microprocessor through NAND gate U9D. NAND gate U9Ds $\overline{INTA}$ input is not used in this design. When $\overline{RD}$ is active (low), the eight buffers are enabled to allow bus data to be input to the microprocessor. The rest of the time these buffers are tri-state. The opposite buffers are then enabled to allow data to be output from the microprocessor to the bus.

1.7.1.6 Address Latch (U5, U6)

High-speed CMOS U5 and U6 are octal D-type flip-flops. The data on the inputs of U5 and U6 contain the low-order and high-order address portion of the bus cycle. When ALE goes low indicating a valid address on the bus, this signal is inverted by U9C. The resultant positive-going edge, when applied to the clock inputs of U5 and U6, clocks the D inputs to the Q outputs. These outputs remain in this state until the next bus ALE cycle. This demultiplexes the address from the data portion of AD0-AD7 (low-order) lines and provides a bus cycle of equal duration on the A8-A15 (high-order) bus address lines. The EN input is tied to the HLDA output of the microprocessor and is not used in this design.

1.7.1.7 Address Decoders (U7, U8)

Table 1-8 is a truth table for U7, the high-order address decode operation, and **Table 1-9** is the truth table for U8, the low-order address decode operation. When enabled by applying a high to input G1 and a low to inputs G2A and G2B, these decoders provide a low logic level on one of seven Y outputs.

The U7 inputs are the most significant four bits of the address bus A12 through A15. A15 must always be low in order for either of these devices to be enabled. U7 outputs, Y0-Y4, are enabled for ROM1, U8 enables G2B (necessary for frequency and BFO data latch strobes), RAM, and ROM2.

Table 1-8. U7 Truth Table

Inputs						Outputs					
Enable			Select								
G1	G2B	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	
VCC	GND	A15	A14	A13	A12						
1	0	0	0	0	0	0	1	1	1	1	
1	0	0	0	0	1	1	0	1	1	1	*
1	0	0	0	1	0	1	1	0	1	1	
1	0	0	0	1	1	1	1	1	0	1	
1	0	0	1	0	0	1	1	1	1	0	

Table 1-9. U8 Truth Table

Inputs						Outputs					
Enable			Select								
G1	G2B	G2A	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5
$\overline{WR}$	*U7Y1	A4-A5	A2	A1	A0						
1	0	0	0	0	0	0	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1
1	0	0	1	0	0	1	1	1	1	0	1
1	0	0	1	0	1	1	1	1	1	1	0

The U8 inputs are the three least significant address bits of the bus, address bits 4 and 5, Y1 decode output from U7, and $\overline{WR}$. Any microprocessor write cycle, to address 1x3x, causes G2A and G2B to be low and G1 to be high through Nand gates U9B and U9A. The U8 outputs Y0-Y5 are clock strobes which latch bus data into the write-only registers used for storing frequency data for the LO synthesizers and BFO synthesizers. **Table 1-10** lists the binary equivalent of the four hexadecimal address digits, 1030 through 1035.

Table 1-10. Addresses 1030 Through 1035

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U16	0 0 0 1	0 0 0 0	0 0 1 1	0 0 0 0
U15	0 0 0 1	0 0 0 0	0 0 1 1	0 0 0 1
U14	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 0
U13	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 1
U12	0 0 0 1	0 0 0 0	0 0 1 1	0 1 0 0
U17*	0 0 0 1	0 0 0 0	0 0 1 1	0 1 0 1

* Used on COR and 1 Hz option.

NOTE: Data Lines 0-7 = AD0-AD7
Data Lines 8-15 = A8-A15

The 26-bit RF frequency data words are provided in **Table 1-11** and the 12-bit BFO frequency data words are provided in **Table 1-12.**

Table 1-11. RF Frequency Data Words

Frequency Digit	10^1	10^2	10^3	10^4	10^5	10^6	10^7
Frequency Bits	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0, 2^1
Register Outputs	Q7-Q4	Q3-Q0	Q7-Q4	Q3-Q0	Q7-Q4	Q3-Q0	Q7, Q6
Register	U16	U16	U15	U15	U14	U14	U13

Table 1-12. BFO Frequency Data Words

	Sign		Frequency Digit		
Frequency Data	+	-	10^1	10^2	10^3
Frequency Bit	NA		2^3-2^0	2^3-2^0	2^3-2^0
Register Outputs	Q5	Q4	Q3-Q0	Q7-Q4	Q3-Q0
Register	U13	U13	U13	U12	U12
NOTE: NA denotes not applicable.					

1.7.1.8 **Frequency Registers (U12-U17)**

U12 through U17 are octal D-type flip-flops and are identical to the U5 and U6 latches described previously, except they are standard CMOS parts. These registers serve as latches for the receiver LO synthesizer and BFO synthesizer circuit.

The clock input to each register is tied to one of the Y outputs of decoder U8. When a hexadecimal address between 1030 and 1035 is on the data bus and a write cycle is executed, one of the Y outputs goes low for the duration of the inverted write input on G1. This positive-going edge of the Y output causes its data on the bus to be clocked from the D input to the Q output. These signals are then used by the necessary inputs to its LO and BFO circuits.

1.7.2 TYPE 794308-1 IF INTERFACE (MFP-A2)

The IF Interface Board replaces the Front Panel Interconnect (A6A2) in the WJ-8718 HF Receiver. The devices on the IF Interface Board allow the microprocessor to read the status of the front panel switches associated with the IF functions. These functions include gain mode, bandwidth, detection mode, RF gain, signal strength, and phone level. The IF Interface Board also switches the audio at the front panel phones jack from combined audio to single sideband audio in the ISB detection mode.

The IF Interface Board is powered by regulated voltages of +5, -15, and +15 Vdc and an unregulated 10 Vdc. The capacitive network formed by C8 through C11 prevents ac ripple and voltage spikes.

Figure 1-10 is a simplified block diagram and **Figure 1-20** is the schematic diagram for the 488-A2 board.

1.7.2.1 Bidirectional Bus Transceiver (U20)

Transceiver U20 is made up of 16 high speed CMOS buffer devices. Only eight buffers are enabled at one time. The direction, or the specific buffers that are enabled, is controlled by the DIR input at pin 1. The pin 1 input is connected to the $\overline{RD}$ line through U13B and U19A for any address decode of 101X (through U10D) or 103X (through U10A). Refer to **Table 1-13** for additional 101X addressing information. The 103X decoder is used for enabling and disabling devices on the board that interface with the front panel. Refer to **Table 1-14** for additional 103X addressing information.

When the $\overline{RD}$ is active for one of the decoded addresses, the buffers are enabled to allow data to be transferred from the board to the external circuits. In all other cases, these buffers are disabled and their opposites are enabled to allow data transfer from the external circuit to the board.

1.7.2.2 Address Latch (U8)

The data on the inputs to U8 contain the low order address portion of the bus cycle from Transceiver U20. When ALE goes low, indicating a valid address on the bus, this signal is inverted by U10B. The resultant positive-going edge when applied to the clock input of U8 latches the data into the Q outputs. These outputs remain in this state until the next ALE cycle. This demultiplexes the address from the data portion of AD0-AD7 low order lines.

1.7.2.3 Decoder Select (U11)

Decoder select U11 is only enabled during a microprocessor read or write cycle to one of the selected device addresses listed in **Table 1-13.** As shown in **Table 1-15,** a Y output goes low only when U11 is enabled and a particular 3-bit code is on the select inputs. A Y output of U11 goes low to enable data to be input or output to the microprocessor data bus. The Y0 through Y3 and Y7 outputs are connected to write-only devices. The Y5 and Y6 outputs are connected to tri-state read-only devices. The Y5 and Y6 outputs are connected to tri-state read-only devices. Output Y4 is connected to both read-only and write-only devices.

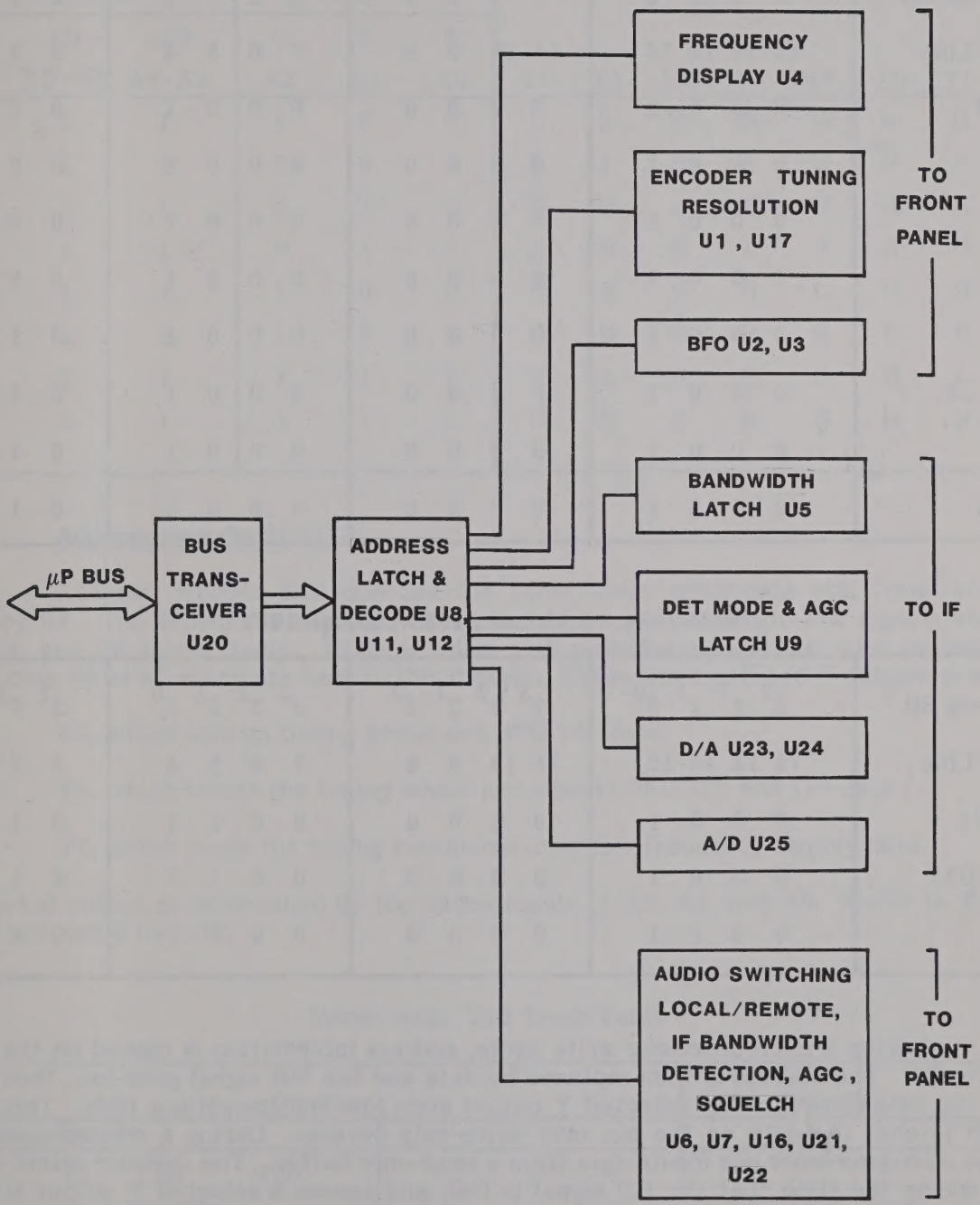
FREQUENCY DISPLAY U4
ENCODER TUNING RESOLUTION U1 , U17
BFO U2, U3
TO FRONT PANEL
BANDWIDTH LATCH U5
DET MODE & AGC LATCH U9
D/A U23, U24
A/D U25
TO IF
μP BUS
BUS TRANS-CEIVER U20
ADDRESS LATCH & DECODE U8, U11, U12
AUDIO SWITCHING LOCAL/REMOTE, IF BANDWIDTH DETECTION, AGC , SQUELCH U6, U7, U16, U21, U22
TO FRONT PANEL

Figure 1-10. IF Interface Board, Simplified Block Diagram

Table 1-13. Addresses 1010 through 1017

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U21B	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
U5	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 1
U9	0 0 0 1	0 0 0 0	0 0 0 1	0 0 1 0
U23	0 0 0 1	0 0 0 0	0 0 0 1	0 0 1 1
U25	0 0 0 1	0 0 0 0	0 0 0 1	0 1 0 0
U16, U6	0 0 0 1	0 0 0 0	0 0 0 1	0 1 0 1
U7	0 0 0 1	0 0 0 0	0 0 0 1	0 1 1 0
U21A	0 0 0 1	0 0 0 0	0 0 0 1	0 1 1 1

Table 1-14. Addresses 1035 through 1037

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U4, U1	0 0 0 1	0 0 0 0	0 0 1 1	0 1 0 1
U17, U3	0 0 0 1	0 0 0 0	0 0 1 1	0 1 1 0
U2	0 0 0 1	0 0 0 0	0 0 1 1	0 1 1 1

During a microprocessor write cycle, address information is placed on the bus and latched by U8. The address is then replaced by data and the WR signal goes low, then high, to indicate the data is valid. The selected Y output goes low and transitions high. This positive transition latches the data on the bus into write-only devices. During a microprocessor read cycle, the microprocessor bus inputs data from a read-only buffer. The decoder select becomes enabled during the time that the RD signal is low, and causes a selected Y output to go low. This low enables an input buffer tri-state output to become active panel information on the data bus for the microprocessor to read.

Table 1-15. U11 Truth Table

Inputs						Outputs							
Enable			Select										
E1	G1	G2B	C	B	A								
A12	$\overline{RD}+\overline{WR}$	A4·A5	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	0	0	0	L	H	H	H	H	H	H	H
H	L	L	0	0	1	H	L	H	H	H	H	H	H
H	L	L	0	1	0	H	H	L	H	H	H	H	H
H	L	L	0	1	1	H	H	H	L	H	H	H	H
H	L	L	1	0	0	H	H	H	H	L	H	H	H
H	L	L	1	0	0	H	H	H	H	H	L	H	H
H	L	L	1	1	0	H	H	H	H	H	H	L	H
H	L	L	1	1	1	H	H	H	H	H	H	H	L

1.7.2.4 **Address Decoder (U12)**

Address decoder U12 decodes the three least significant bits from the address latched by U8. The decoder is enabled when a logic high and two logic low signals are applied to E1, G1, and G2 respectively. When enabled, U12 provides a logic low level on one of eight outputs (only three of which are used in this design). These three utilized Y outputs are:

Y5, which selects tuning wheel and BFO 10^1 data

Y6, which resets the tuning wheel and selects BFO 10^2 and 10^3 data

Y7, which reads the tuning resolution or writes frequency display data.

The selected output is determined by the coded inputs at A2, A1, and A0. Refer to **Table 1-16** for the truth table for U12.

Table 1-16. U12 Truth Table

Inputs						Outputs		
Enable			Select					
E1	G1	G2B	C	B	A			
A12	$\overline{RD}+\overline{WR}$	A4·A5	A2	A1	A0	Y5	Y6	Y7
H	L	L	1	0	1	L	H	H
H	L	L	1	1	0	H	L	H
H	L	L	1	1	1	H	H	L

1.7.2.5 Frequency Display Register (U4)

The RF frequency display register is an octal D-type flip-flop, used to output the frequency data in BCD and the display digit position in binary. Refer to **Table 1-17** for the frequency display data word. The RF frequency display is multiplexed through the software in the main program. The microprocessor periodically outputs a byte of data containing the RF digit and display position. This continuous output to each display position keeps all the digits illuminated. Writing data to U4 occurs when address 1037 is on the data bus. This address selects the Y7 output of decoder U12.

The microprocessor then loads the frequency data byte on the bus. The microprocessor write line transitions high which disables U12 and causes a low-to-high transition on the clock input of U4. This latches the data on the D inputs of U4 to its Q outputs.

Table 1-17. Frequency Display Data Word

U4 Output	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Display Signal	2^3	2^2	2^1	2^0	QØ	Q1	Q2	N/U
	10^1 digit				0	0	0	
	10^2 digit				0	0	1	
	10^3 digit				0	1	0	
	10^4 digit				0	1	1	
	10^5 digit				1	0	0	
	10^6 digit				1	0	1	
	10^7 digit				1	1	0	
	Not Used				1	1	1	

1.7.2.6 Tuning Wheel Register (U17)

Integrated circuit U17 is a 4-bit D-Type flip-flop register with tri-state outputs (only two of the flip-flops are used in this application). The flip-flop outputs, Q1 and Q2, tell the microprocessor if the front panel tuning wheel is being rotated and, if so, in which direction: clockwise to increase the displayed frequency (at the selected step size) or counterclockwise to decrease the frequency.

Table 1-18 is the U17 truth table. The table shows that the levels at the D inputs transfer to the Q outputs on the positive-going transition of the clock pulse when G1, G2, and CLR are low; in addition the Q outputs must be enabled by low levels on the OD1 and OD2 inputs. A high level on the CLR input resets the flip-flops and all Q outputs go low.

Table 1-18. U17 Truth Table

Inputs					Output
CLR	CLK	G1	G2	D	Q
H	X	X	X	X	L
*L	L	X	X	X	Q0
*L	↑	H	X	X	Q0
L	↑	X	H	X	Q0
L	↑	L	L	L	L
L	↑	L	L	H	H

*denotes a stead-state condition.

NOTES: 1. Q0 denotes level of Q before the steady-state condition was established.
2. When inputs OD1 and OD2 are high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flop is not affected.

The low levels required to allow data at the D inputs to be clocked to the Q outputs are provided as follows:

1. G1 and G2 are tied to ground.

2. 0D1 and OD2 are low when U13C goes low or when the hexadecimal address 1035 has been on the microprocessor address/data bus and latched by U8.

3. CLR is the inverted (by U18F) level on Y6 of U12. When U17 is addressed, only one of output (Y5) is low, all others are high. Therefore, CLR is low when U17 is addressed by the microprocessor. When CLR goes high, the Q outputs of U17 are reset. The processor resets U17 by a $\overline{RD}$ to address 1036.

In summary, the U17 outputs (Q1 and Q2) reflect the data on the D1 and D2 inputs when the microprocessor addresses U17 at address 1035 and initiates a read operation. The D1 input is tied high to +5 Vdc. This high level will be clocked to the Q1 output the first time the CLK input transitions high and Q1 will remain high until U17 is reset (CLR high). A high level at Q1 is evidence that the CLK has transitioned high. The CLK input is the inverted (U18D) CLK output of optical encoder (A7U1).

The optical encoder converts the rotation of the front panel tuning wheel into electrical pulses and outputs two trains of square wave pulses (on the CLK and DIR lines) which are applied to the Manual Tuning Module (A7). The trains of pulses are phase-related to the direction of tuning wheel rotation; DIR leads CLK if the rotation is clockwise, as shown in **Figure 1-11**, and lags CLK if the rotation is counterclockwise, as shown in **Figure 1-12.**

The Q1 output of U17 is high only when CLK transitions are high. This happens only when the front panel tuning wheel is rotated (and CLR is low). The microprocessor addresses U17 for a read operation approximately every 5 milliseconds during the execution of

its program and "examines" the Q1 output (on the LSB of the data bus). If Q1 is low, the processor knows that the tuning wheel is not rotated and continues with the execution of its program.

If the microprocessor finds that Q1 is high, the tuning wheel is being rotated and the processor examines the Q2 output (on the AD1 data bus line) to determine the direction of rotation. At the same time the positive CLK transition transferred the D1 input level to Q1, the D2 input level transferred to Q2. D2 is the inverted (by U18E) DIR line pulse train from the optical encoder. **Figures 1-11** and **1-12** illustrate the timing for the clockwise and counterclockwise rotation of the tuning wheel. If the direction is clockwise, the D2 input is high each time the U17 CLK transitions high; therefore, Q2 will go high (if it was low at the first rising clock edge) and remain high until U17 resets or until the direction of rotation changes. If the direction is counterclockwise, the D2 input is low each time the U17 CLK transitions high; Q2 will either be low from the time of U17 reset and will remain low, or will be high from clockwise rotation and will go low at the first rising clock edge.

The sequence of the microprocessor program is such that following a $\overline{RD}$ of U17, the processor addresses 1036 and output U12Y6 goes low. This low level is inverted by U18F and CLR goes high, resetting the Q1 and Q2 outputs to a low level. The reset procedure ensures that a high level on Q1 indicates that the tuning wheel has been rotated since the last time Q1 was examined and, furthermore, because only 5 milliseconds has elapsed, the tuning wheel is still being rotated and the microprocessor can proceed to increment or decrement the displayed frequency.

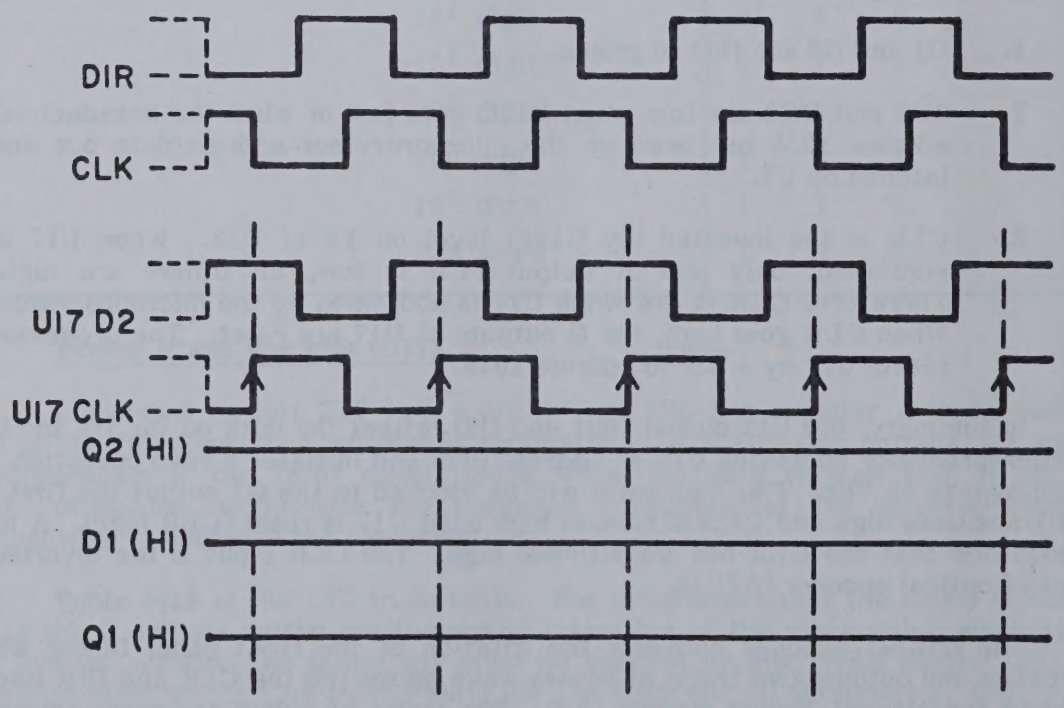

Figure 1-11. Timing Diagram for Tuning Wheel Clockwise Rotation

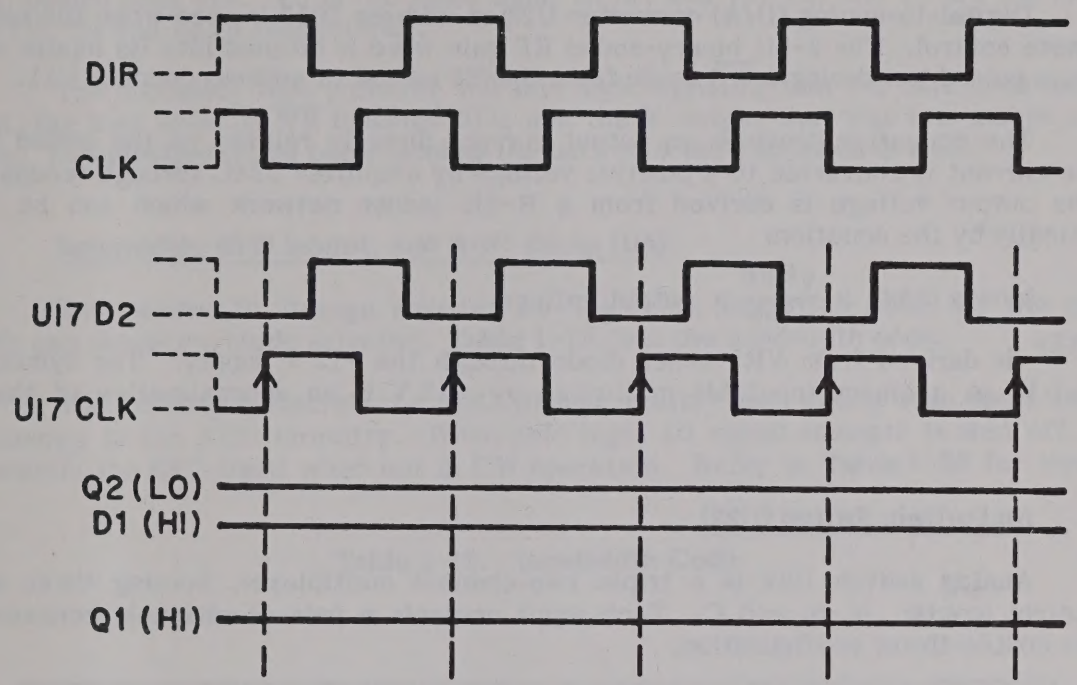

Figure 1-12. Timing Diagram for Tuning Wheel Counterclockwise Rotation

1.7.2.7 **Tuning Resolution (U1)**

Tri-state buffer (U1) is used to input the selected tuning rate data from the front panel. The U1 outputs are enabled when the output of OR gate U13D goes low. This occurs when a RD and a hexadecimal address of 1037 is placed on the data bus, selecting the Y7 output from U12 decoder. The microprocessor then inputs the select data and uses this information when the RF frequency is incremented or decremented.

1.7.2.8 **BFO Frequency Buffers (U2, U3)**

Hex buffer U2 and octal buffer U3 are both tri-state buffers. Buffer U2 inputs the BFO ± sign and the optional 10^1 Hz BFO frequency data from the front panel. Buffer U3 inputs the 10^2 Hz and 10^3 Hz BFO frequency data.

When the microprocessor places a hexadecimal address of 1035 on the data bus and executes a read cycle, the Y5 output of decoder U12 goes low enabling the U2 buffer through U13C. This causes the U2 buffer outputs to be placed on the data bus for the microprocessor to input. Similarly, when a hexadecimal address of 1036 is placed on the data bus, the U12 output Y6 to go low and enables tri-state buffer U3. This causes the tri-state outputs of U3 to be actively placed on the data bus.

1.7.2.9 RF Gain Conversion D/A (U23)

Digital-to-analog (D/A) converter U23 at address 1013 is used when the receiver is under remote control. The 8-bit binary-coded RF gain word is latched into its inputs when the WR1 input is pulsed low during a $\overline{WR}$ cycle from the Y3 output of address decoder U11.

The converter provides an output current directly related to the coded RF gain word. The current is converted to a positive voltage by amplifier U24C through feedback input RFB. The output voltage is derived from a R-2R ladder network which can be deduced mathematically by the equation:

$$\text{binary input} \times \frac{V^{REF}}{256} = \text{output voltage.}$$

Where V^{REF} is derived from VR1 zener diode through the -15 V supply. The symbol V^{REF} equals -5.1 V, so a binary input bit multiplied by .019 V is an approximation of the output voltage.

1.7.2.10 Audio/Gain Switch (U22)

Analog switch U22 is a triple two-channel multiplexer, housing three separate digital control inputs: A, B, and C. Each input controls a pair of channels connected in a single-pole double-throw configuration.

Input A controls channel X which selects the RF gain voltage. Input A is tied to the remote/local latch U21B. When the receiver is in the local mode, the A input is held low and the RF gain potentiometer voltage is fed through channel X0 to X. When the receiver is in the remote mode, the A input is held high and the digital-to-analog RF gain voltage is fed through channel X1 to X.

Input B controls the output of the manual RF gain voltage. When manual AGC is selected, input B is held high and the voltage from channel X is output to the amplifier U24D through channel Y1 to Y. When the receiver is in either fast or slow AGC, input B is held low and the RF gain voltage is turned off by the ground on channel Y0 to Y.

Input C controls the audio output connected to the PHONES jack. In any detection mode but ISB, the audios on the ring and tip of the front panel stereo PHONES jack are the same. In ISB detection mode, U22 switches the audio so that the USB audio is on the tip of the jack and LSB audio is on the ring, allowing both audios to be monitored with a 600 ohm stereo headphone. Input C is held high by the latch U9 ISB output, connecting the ISB audio to feed through channel Z1 to Z.

1.7.2.11 Registers (U5, U9, U21)

Three registers serve as storage devices for the control of the IF section of the receiver. Each register latches the data on its D inputs to the Q outputs on a positive-going transition of its clock pulse.

To initiate a write operation, the microprocessor places the address of the device on the data bus and issues the ALE signal, latching the lower-order bits of the address into U8. The processor pulls the $\overline{WR}$ line low and address decoder U11 is enabled. U11 decodes the

address latched by U8, and the Y output connected to the clock or clock pulse input of the addressed device goes low. Y0 is the clock input U21B, and Y1, Y2, and Y7 are the clock pulse inputs to U5, U9 and U21A respectively.

The processor then pulls the $\overline{WR}$ line high, signaling that the data is on the bus. At this point, the high level on $\overline{WR}$ disables U11, and the Y output that was low makes a positive transition. This positive-going pulse latches the data into the addressed device.

1.7.2.12 Bandwidth, BFO Inhibit, and AGC Dump (U5)

The bandwidth storage register U5 holds the bandwidth code for the particular bandwidth and detection mode selected. **Table 1-19** lists the bandwidth code.

The Q5 output controls the AGC Dump circuitry used during scan operation to hold off any energy in the AGC circuitry. When held high, all signal strength is shut off. The Q7 output inhibits the BFO input when not in CW operation. Refer to **Table 1-20** for the U5 data word.

Table 1-19. Bandwidth Code

Selected Bandwidths	16 kHz	6 kHz	3.2 kHz	1 kHz	.3 kHz
Active U5 Outputs	Q6 Q4	Q6 Q3	Q6 Q2	Q2 Q1	Q2 Q0

Table 1-20. Address 1011 (U5) Data Word

Output	Function
Q7	BFO Inhibit
Q6	16 kHz (A) IF Bandwidth
Q5	AGC Dump
Q4	16 kHz (B) IF Bandwidth
Q3	6 kHz IF Bandwidth
Q2	3.2 kHz IF Bandwidth
Q1	1 kHz IF Bandwidth
Q0	.3 kHz IF Bandwidth

1.7.2.13 Gain/Detector Mode (U9)

Table 1-21 lists the data word for U9. The microprocessor updates receiver gain and detection mode parameters by writing the data into register U9. The Q outputs connect to the detection mode and AGC circuits in the IF section of the receiver. A high logic level indicates the selected gain or detection mode and activates the IF circuit to initiate the parameter change.

Table 1-21. Address 1012 (U9) Data Word

Output	Function
Q7	SLOW AGC
Q6	MAN AGC
Q5	LSB
Q4	ISB
Q3	USB
Q2	CW
Q1	FM
Q0	AM

1.7.2.14 Local/Remote Select (U21B)

Register U21B (address 1010) provides a select level to gain voltage switch U22. The microprocessor reads the status of the front panel tuning disable switch, during a read operation on the front panel Manual Tuning Module (A7), to determine if the receiver is in the local or remote operating mode. The local/remote status is contained in the LSB of the local/remote data byte in a remote monitor operation. The bit is low if the receiver is in local mode and high if the receiver is in remote mode. The logic level is applied to the D input of the flip-flop U21B via data line AD0. The bit level is latched to the Q output of U21B when the clock input makes a positive transition. From U21B, the pulse representing the local/remote code is applied to the select input of U22. U22 switches between manual and remote RF gain voltage.

1.7.2.15 AUDIO ON/OFF (U21A, U16A, U16B)

Register U21A (address 1017) provides a select level to analog switches U16A and U16B which, in turn, provide audio squelching during scan operation. The output of U21A is low in normal operation allowing both audio channels to be routed to the front panel. During scan operation, the microprocessor provides a high level on the AD7 input to the register. The bit is latched to the Q output on the positive-going transition of the clock input. When their select inputs are held high, U16A and U16B become an open circuit and provide a squelched audio output.

1.7.2.16 A/D Converter (U25)

Analog-to-digital converter U25 (address 1014) is made up of an eight-channel, multiplexed analog switch, an 8-bit A/D converter, address decode circuitry, and a tri-state output buffer.

Only one of the eight channel inputs to the multiplexer is used in this design. Signal strength is monitored if scan, COR, or remote operation is being utilized.

To select the signal strength input (IN2), a select address code of "0, 1, 0" must be written to the C, B, and A inputs, respectively, of the A/D converter. To select a channel, the address lines are latched into the address decoder by the low-to-high transition of the A/D ALE input. The A/D ALE input goes low when a $\overline{WR}$ to address 1014 occurs and decoder U11 output Y4 goes low. When the $\overline{WR}$ signal returns to a high state, the output of U19C transitions high, latching in the address data into the address decoder.

After a channel has been selected, the data can be read from the output buffer by placing a microprocessor read instruction to address 1014 on the bus. This causes decoder U11 output Y4 to go low, as well as the output of U19D. The low from U19D is then inverted by U14C to enable the tri-state output buffer of the A/D converter. This places the conversion data in the buffer onto the bus for the microprocessor to accept.

The converter is the heart of the single-chip multiplexed A/D. The converter comprises three major parts: the 256R ladder network, a successive approximation register (SAR), and a comparator. Continuous conversion is accomplished by tying the EOC (end of conversion) output to the ST (start conversion) input. The SAR is reset on the positive edge of the ST pulse and initiates conversion on the falling edge. A reset is applied on power-up through U19B to the ST input, to ensure conversion start.

All analog inputs are referenced to Vcc (+5 V). The binary output is derived by the equation:

$$\text{binary output} = \frac{V_{IN}}{V_{REF}} \times 256$$

Clock circuit U18B and U18C provide timing and control of the A/D conversion rate. Circuit U18B is configured as an RC oscillator that provides an approximately 700 kHz clock that is conditioned by U18C before entering the A/D clock input.

1.7.2.17 Analog Inputs

Signal strength input, IN2, is the only input used in this design. The other inputs exist for future development. The IN2 signal strength input is taken from the AGC circuit, inverted and amplified by U24A. Potentiometer R7 sets the multiplication ratio along with R8. Refer to **paragraph 1.8.3.1** for R7 adjustment procedures. MAN signal strength is also passed through isolation amplifier U24B to protect the meter circuit from interfering with the AGC signal strength circuit.

1.7.3 TYPE 796075 I/O INTERFACE (488-A3)

The 488-A3 board interfaces the microprocessor in the receiver's control block with the remote control equipment. All board components are powered by +5 Vdc, applied across bypass capacitors C2 through C5. Refer to **Figure 1-21**, Type 796075 I/O Interface Schematic Diagram.

1.7.3.1 Address Latch (U6)

Integrated circuit U6 is an octal D-Type flip-flop. The clear (CLR) input is held high by Vcc, causing information at the D inputs to be latched to the Q outputs on the positive-going edge of the clock pulse. The clock pulse to U6 is the microprocessor control line ALE, inverted by U8E. ALE goes low, and is inverted when a valid address has been placed on the data bus. The resultant positive-going clock pulse to U6 latches the lower-order address bits to the Q outputs. From the outputs of U6, four of the address bits are decoded as necessary to clock or enable the addressable circuits on the I/O board: U1, discussed in **paragraph 1.7.3.6**, and U4, discussed in **paragraph 1.7.3.4**. The three least significant bits of the address are described in **paragraph 1.7.3.6.1**.

1.7.3.2 Address Decoder (U7)

Integrated circuit U7 is a three-to-eight line decoder, enabled by one high and two low logic levels on the G inputs, as shown in **Table 1-22**. When U7 is enabled, the three select inputs at A, B, and C are decoded and one of the eight outputs goes low.

Table 1-22. U7 Truth Table

Inputs						Outputs		
Enable			Select					
G1	G2A	G2B	A	B	C	Y0	Y1	Y2
H	L	L	L	L	L	L	H	H
H	L	L	L	L	H	H	L	H
H	L	L	L	H	L	H	H	L

1.7.3.2.1 U7 Enable

The G1 enable input to U7 is the A12 data line. **Table 1-23** lists the addressable devices on the I/O board. The A12 bit is high when the least significant bit of the MSD of the hexadecimal address is 1 (0001). G2B is the inverted (by U8A) level of the AD5 address bit. To provide the two low levels to enable U7, AD5 must be high and AD4 must be low. As shown in **Table 1-23**, the enabling conditions exist when one of the hexadecimal addresses 1020, 1028 through 102F, or 1060 has been placed on the data bus.

Table 1-23. Addresses 1020, 1028 Through 102F, and 1060

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 0 0 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 0 0 1
U1	0 0 0 1	0 0 0 0	0 0 1 0	0 0 1 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 0 1 1
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 1 0 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 1 0 1
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 1 1 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	1 1 1 1
U4	0 0 0 1	0 0 0 0	0 0 1 0	0 0 0 0
U10	0 0 0 1	0 0 0 0	0 1 1 0	0 0 0 0

NOTE: Data Lines 0-7 = AD0 - AD7
Data Lines 8-15 = A8 - A15

1.7.3.2.2 **U7 Select**

The select input A to U7 is the address bit carried on the AD3 data line. (Note that the three least significant bits of the address, carried on AD0 through AD2, are not decoder inputs. These bits have a unique use and are discussed in **paragraph 1.7.3.6.1.**

Three of the eight available outputs of U7 are used to enable the addressable devices on the I/O board. Comparison of **Tables 1-22** and **1-23** shows that the Y1 output goes low when one of the eight U1 addresses is latched by U6, and Y0 goes low when the U4 address is latched, Y2 goes low when U10 is addressed.

1.7.3.3 **Switch Assembly (S1)**

The eight-position switch assembly (S1) is used, prior to remote operation, to establish receiver address. A high logic level indicates a closed switch, and a low logic level indicates an open switch. **Paragraph 1.4.2**, part of the preparation for 488 operation procedure, contains a description of the switch settings.

1.7.3.4 Tri-State Buffer/Inverter (U4)

Octal tri-state buffer U4 allows the microprocessor to read the settings of the S1 switch assembly. The buffer inputs the logic levels of the switch settings from the pull-up resistive network, U5. The outputs of U4 are tri-stated if the logic levels at the enable inputs (pins 1 and 19) are high. When the enable inputs go low, the outputs of U4 are taken out of tri-state and the data from the S1 switch assembly are inverted and placed on the lower-order address/data bus lines. U4 is enabled when the $\overline{RD}$ signal from the microprocessor goes low (after the address is latched) and when U7Y0 is low. As discussed in **paragraph 1.7.3.2.2**, U7Y0 is low only when address 1020 is latched by U6.

The microprocessor initiates a read operation to address 1020 (U4) and loads the equipment address into U1. The 488M-A3 interface device (U1) is programmed by the microprocessor to determine if the address on incoming data matches the switch-established address.

1.7.3.5 Transceiver Network (U2 and U3)

Bidirectional bus transceivers, U2 and U3, are octal transmitter/receivers which interface the TTL logic of U1 with the IEEE-488 Bus. Either the transmitter or receiver in each of the eight channels in both U2 and U3 is enabled, forcing the disabled channel to a high impedance state.

Transceiver U2 interfaces the DIO data lines. When the signal level at pin 1 is high, data on the DIO lines transfer from the D to B ports and, when low, from the B to D.

Transceiver U3 interfaces the handshake and management control signals. The levels on the TE (Talk Enable) and DC (Direction Control) inputs, as well as the bus signal ATN, determine the direction of signal flow. (See **Table 1-3** for an explanation of the handshake and management control line abbreviations used in the following discussion.)

TE controls the direction of DAV, NDAC, and NRFD. When TE is high, DAV=T, NDAC=R, and NRFD=R (T = transmit; R = receive).

DC controls the direction of IFC, REN, SRQ, and ATN. When DC is high, IFC = R, REN = R, SRQ = T, and ATN = R.

ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI, whenever the TE and DC inputs are in the same state.

1.7.3.6 GPIB (General Purpose Interface Bus), (U1)

The GPIB (IEEE-488) Interface, U1, is a peripheral device designed to interface the microprocessor in the receiver control block with the IEEE-488 bus. Functions of the GPIB Interface include data transfer, handshake protocol, talk/listen addressing procedures, device clearing and triggering, service requests, and both serial and parallel polling schemes. Refer to **Figure 1-13**, the GPIB Interface Block Diagram to correlate the following functional descriptions of U1 components.

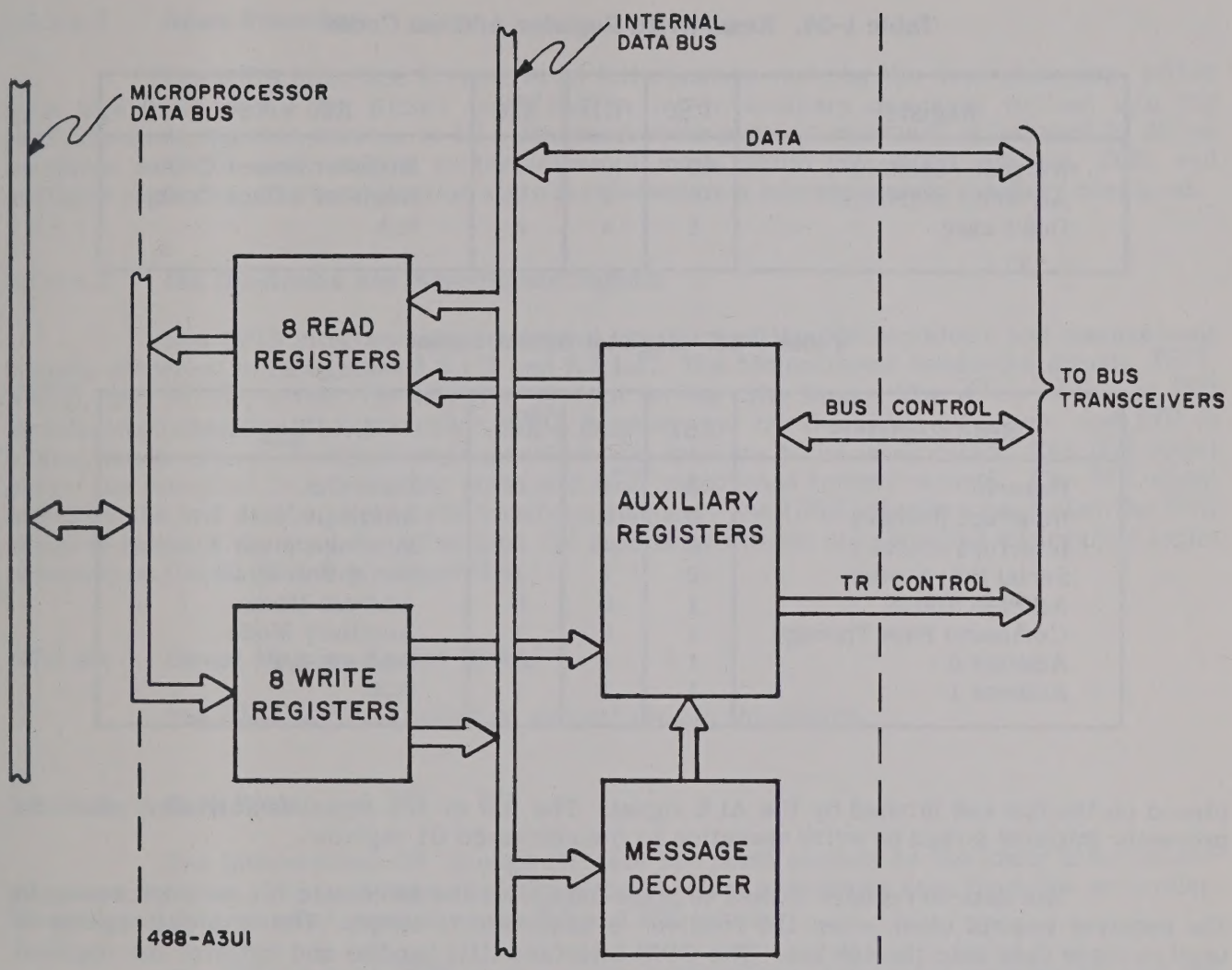

Figure 1-13. GPIB Interface (U1) Block Diagram

1.7.3.6.1 Read/Write Registers

The GPIB Interface structure includes eight registers that the microprocessor writes to, and eight registers that the processor reads from. One read register and one write register are used for the transfer of data. The remaining write registers are used by the microprocessor to establish operating characteristics of U1. The remaining read registers provide the processor with a monitor of bus and controller conditions.

The registers are accessed by the levels on the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and RS0 through RS2 lines as listed in **Table 1-24. Table 1-25** lists the RS0 through RS2 codes and functions of the read/write registers. The RS0 through RS2 codes are established by the three least significant bits of the address on the microprocessor bus lines. The $\overline{CS}$ signal level is established by decoding other address bits, as described in **paragraphs 1.7.3.1** and **1.7.3.2.** The $\overline{CS}$ signal goes low to enable U1 when a hexadecimal address between 1028 and 102F (**Table 1-23**) has been

Table 1-24. Read/Write Register Address Codes

Register	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	RS0 - RS2
All read registers	0	0	1	Register Select Code
All write registers	0	1	0	Register Select Code
Don't care	1	x	x	xxx

Table 1-25. Register Select Codes

Read Registers	RS2	RS1	RS0	Write Registers
Data-In	0	0	0	Data-Out
Interrupt Status 1	0	0	1	Interrupt Mask 1
Interrupt Status 2	0	1	0	Interrupt Mask 2
Serial Poll Status	0	1	1	Serial Poll Mode
Address Status	1	0	0	Address Mode
Command Pass Through	1	0	1	Auxiliary Mode
Address 0	1	1	0	Address 0/1
Address 1	1	1	1	EOS

placed on the bus and latched by the ALE signal. The $\overline{RD}$ or $\overline{WR}$ signal is activated when the processor initiates a read or write operation to the addressed U1 register.

The data-in register is used to move data from the 488 bus to the microprocessor in the receiver control block when the receiver is addressed to listen. The data-out register is used to move data onto the 488 bus. The GPIB Interface (U1) handles and initiates the required handshake protocol.

The write interrupt mask registers are configured by the microprocessor to select the events that will cause an interrupt signal to be generated by the corresponding bit in the interrupt status registers. The status registers are read by the microprocessor to determine which event has occurred so that the proper service routine can be executed.

The address mode register is used by the microprocessor to configure the addressing mode, establishing the way that the information in the address 1 and 0 registers is used. The configuration of addressing is such that processor intervention is not required to recognize addressing by the controller. The address 0/1 register determines the talker or listener functions. The address status register is used for monitoring the address state.

The remaining registers provide the means for the processor to establish and monitor U1 operating characteristics which include requests for service, decoding of incoming messages, loading of "hidden" U1 auxiliary registers, auxiliary commands, delays and finishes to handshake signals, internal time delays on the data lines, and parallel/serial poll protocol.

1.7.3.6.2 Reset Procedure

The GPIB Interface is reset to an initialization state by the microprocessor, either by a high level on the U1 RESET input line or by an auxiliary command written into the auxiliary mode register internal to U1. The reset state pulse or command is followed by initial condition configurations written to the interrupt mask, serial poll mode, address, EOS, and auxiliary registers. The initialization state is released by a microprocessor auxiliary command.

1.7.3.6.3 488 Handshake and Management Signals

The GPIB Interface implements all functions of the 488 handshake and management signals, described in **paragraphs 1.5.1.2** and **1.5.1.3.** The bidirectional handshake signals, $\overline{\text{DAV}}$, $\overline{\text{NRFD}}$, and $\overline{\text{NDAC}}$, effect the transfer of data on the DIO lines. The $\overline{\text{ATN}}$, $\overline{\text{REN}}$, and $\overline{\text{IFC}}$ signals originate from the controller, $\overline{\text{SRQ}}$ is generated by the GPIB Interface, and $\overline{\text{EOI}}$ is bidirectional. The $\overline{\text{ATN}}$ signal level specifies how data are to be interpreted. The $\overline{\text{IFC}}$ signal places the interface in a quiescent state and $\overline{\text{REN}}$ establishes remote control. The $\overline{\text{EOI}}$ signal indicates the end of a multiple byte transfer sequence. The GPIB Interface generates the $\overline{\text{SRQ}}$ signal to indicate the need for attention. All signals on the bus are specified as negative logic; however, on the U1 pins, logic is positive.

1.7.3.6.4 Direct Memory Access (DMA)

The $\overline{\text{DMA}}$ $\overline{\text{ACK}}$ is pulled up and not used in this design.

1.7.3.6.5 Data Ports

The bidirectional D0 through D7 data bus ports connect to the lower order microprocessor data bus. The ports input data from the receiver and output data from the controller. Direction of data transfer depends on the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals.

The $\overline{\text{DI01}}$ through $\overline{\text{DI08}}$ ports transfer bidirectional data bytes between U1 and the external transceiver, U2 (**See paragraph 1.7.3.5**). The direction of transfer depends on the level of control signal TR/1.

1.7.3.6.6 Clock Input

A clock pulse is generated by the RC time constant of R1 and C1 and applied to the clock input. The time constant, coordinated with the feedback and inversion characteristics of U8B and F, provides square wave pulses of 1 MHz to a time delay generator internal to U1.

1.7.3.6.7 Transmit/Receive Control Lines

The TR/1 signal is generated by U1 to control the operation of the external transceivers, U2 and U3 (**paragraph 1.7.3.5**). The TR/1 signal is set high to indicate output to the 488 bus. Data/signals are on the DI01 through DI08, EOI and DAV lines. Input (bus to U1) signals are on the NRFD and NDAC lines. The TR/1 signal is set low to indicate input signals

on the DI01 through DI08, EOI and DAV lines, and output signals on the NRFD and NDAC lines. The TR/2 line is not used.

1.7.3.7 Master/Slave Hand Off (U9, U10)

When the receiver is programmed as a master device, it is necessary to control the ATN bus signal for sending commands over the bus. Register U10 is used to control the DC input of transceiver U3. The DC input determines the direction of the ATN transceiver.

To send a command out over the bus, the U10 register $\overline{Q}$ output is set to a low state to reverse the control of the ATN transceiver channel. By enabling its driver, the ATN input is then held low by R7 which sets ATN active on the GPIB. With ATN active, any data sent through the U2 data buffers is treated as a command instruction by any device connected to the master receiver. Resistors R5 and R6 keep REN and SRQ inactive, while the DC input is in the command state.

When address 1060 is placed on the bus and latched by U6, decoder U7 output is then enabled. During a $\overline{WR}$ bus cycle, the U9D output goes low. On the low-to-high transition at the end of the $\overline{WR}$ cycle, the data (from AD0) on the D input of latch U10 is clocked into the Q output.

The U10 Q output is low during normal operation, allowing the normal ATN signal from U3 to be passed through U9B to U1.

U10 is reset on power-up by the inverted reset signal from U8D.

1.8 MAINTENANCE

The maintenance procedures in **Section IV** of the WJ-8718 HF Series Receiver Instruction Manual can be adapted and applied to a receiver equipped with the WJ-8718/488-2 Option. The procedures should be supplemented with the information contained in **paragraphs 1.8.1** through **1.8.5.2** of this WJ-8718/488-2 Option Instruction Manual; all references to the Type 791828 Front Panel Interconnect and the Type 791575 Manual Up/Down Counter Boards should be considered void.

1.8.1 TEST EQUIPMENT

The WJ-8718/488-2 Option contains a large number of digital integrated circuits (ICs). The most efficient method of testing and troubleshooting digital ICs, in most cases, is to use a Logic Troubleshooting Kit containing probes capable of supplying and detecting digital voltage levels and pulses. A typical set of probes, the Hewlett-Packard 5022A Multi-Family Logic Troubleshooting Kit, is recommended. This kit contains the following devices:

545A	Logic Probe
546A	Logic Pulser
547A	Current Tracer
548A	Logic Clip

The basic functions of these devices are described in **paragraphs 1.8.1.1** through **1.8.1.4.**

1.8.1.1 Logic Probe

The logic probe detects logic levels and pulses without the need for a voltmeter or oscilloscope. The lamp in the probe tip shows a bright light for a logic high, no light for a logic low, and a dim light for a floating or bad logic level. When a pulse train of up to 50 MHz is detected, the lamp blinks at a rate of 10 Hz. Power for the probe is supplied by the unit under test.

1.8.1.2 Logic Pulser

The logic pulser probe provides pulses that are compatible with digital circuits. When the probe tip is placed against a circuit point, the probe senses the logic level present, and when the pulse button is pressed, the circuit is briefly pulsed to the opposite state. By using the logic probe and logic pulser in combination, a known input can be supplied to an IC, and the effect can be observed at the output.

1.8.1.3 Current Tracer

The current tracer probe senses the magnetic field produced by current flow in the circuit. It can be used to trace current from the source to the sink; therefore, it can be helpful in finding short-circuits, or in determining if an IC output is actually sourcing current, and, if so, in finding out where the current is flowing.

1.8.1.4 Logic Clip

The logic clip indicator displays the logic level present at all of the terminals of an IC at the same time. The readout is 16 LEDs that glow if the terminal is high and are dark if the terminal is low. When used in combination with the logic pulser, the effect of input pulses on all of the terminals of the IC under test can be observed.

1.8.2 PERFORMANCE TESTS

Performance tests should be utilized to confirm operating specifications during initial inspection, during periodic checks, or after repairs have been made. A receiver equipped with the WJ-8718/488-2 Option can be tested, in the manual operating mode, using the procedures as outlined in the WJ-8718 HF Series Receiver Instruction Manual. In the remote operating mode, the following guidelines should supplement each test procedure. It is assumed that the proper remote control equipment has been connected to the receiver under test and that the receiver has been prepared for operation per instructions in **paragraph 1.4** of this supplement.

1. Energize the receiver under test and depress the front panel TUNING DISABLE button.

2. Use remote control command instructions (**paragraph 1.5.2**) to establish the receiver parameters listed in step 1 of the test procedure.

3. Proceed to carry out the test procedure instructions, using remote commands to change the receiver parameters as required during the test. If test results are satisfactory, the receiver is responding properly to the remote commands. If a problem becomes evident during a performance test procedure, refer to the troubleshooting section of the WJ-8718 HF Series Receiver Instruction Manual and to **paragraph 1.8.4** of this supplement.

4. Initiate both full- and partial-status monitor operations and verify that the monitored data correspond to the most recently commanded parameters.

NOTE

When the receiver under test is in any sideband mode (ISB, LSB, or USB) the receiver will automatically be forced into the 16 kHz bandwidth.

5. Verify that the receiver status can be monitored with the front panel TUNING DISABLE pushbutton disengaged.

1.8.3 ALIGNMENT PROCEDURES

1.8.3.1 Alignment of Digitized Signal Strength

The digitized signal strength voltage is aligned by adjusting 488-A2R10. To locate the resistor, (R7), consult **Figures 1-17** and **1-20**, location of components and schematic diagrams. To align the voltage, use the following procedure:

1. Connect the test equipment as shown in **Figure 1-14** and energize all equipment.

2. Tune the signal generator to provide a 15.005 MHz, CW signal at +10 dBm.

3. Establish the following receiver parameters, remotely, using an HP 9825A calculator:

Detection Mode	CW
Bandwidth	16 kHz
Gain Mode	AGC FAST
Tuned Frequency	15.005 MHz

4. While monitoring signal strength, adjust R7 for 115 on the calculator.

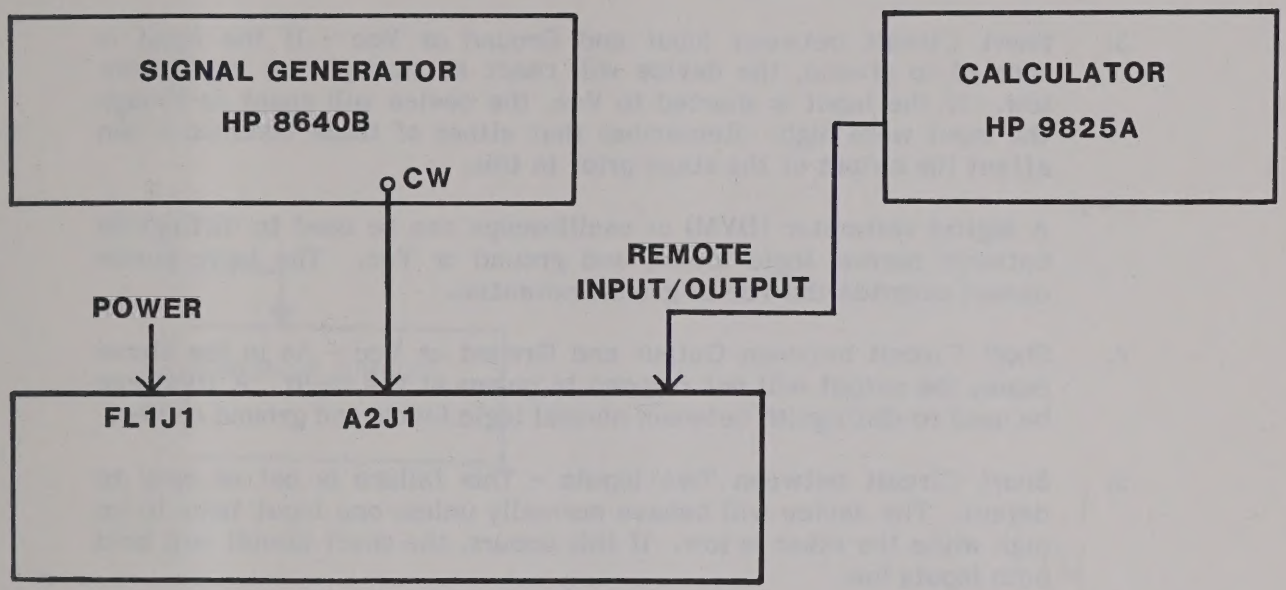

Figure 1-14. Signal Strength Alignment Equipment Setup

NOTE

A monitor program is shown in **Table 1-6** and is described in **paragraph 1.5.2.1.2.**

5. Decrease the drive from the signal generator in 10 dB decrements and verify that the monitored signal strength decreases in value.

1.8.4 TROUBLESHOOTING

Figure 1-15, the WJ-8718/488-2 Option Troubleshooting Tree, will aid in isolating trouble in the digital circuits. General troubleshooting and repair information follows.

1.8.4.1 Symptoms of Integrated Circuit Failure

1. Open Input - The output of a digital IC that has an opened input (internal) will usually behave as if the input level as a static high. The output of this IC will not respond to input pulses.

2. Opened Output - The output level of a digital IC that has an opened output (internal) will not respond to input pulses and will usually assume a faulty level of approximately 1.5 volts. This faulty level

will often have the same effect as a high level on the input of the next IC in the circuit.

3. Short Circuit between Input and Ground or Vcc - If the input is shorted to ground, the device will react as through the input were low. If the input is shorted to Vcc, the device will react as though the input were high. Remember that either of these conditions can affect the output of the stage prior to this.

   A digital voltmeter (DVM) or oscilloscope can be used to distinguish between normal logic levels, and ground or Vcc. The logic pulser cannot override the Vcc or ground potential.

4. Short Circuit between Output and Ground or Vcc - As in the above cases, the output will not respond to pulses at the input. A DVM can be used to distinguish between normal logic levels and ground or Vcc.

5. Short Circuit between Two Inputs - This failure is not as easy to detect. The device will behave normally unless one input tries to go high while the other is low. If this occurs, the short circuit will hold both inputs low.

6. Internal Failure of Logic Circuits - The effect of this trouble is to lock the output in either the high or low state. The output will not respond to input pulses.

1.8.4.2 In-Circuit Tests

Digital ICs rarely have partial or intermittent failures; therefore, the failures may usually be located by simple static tests. The circuit troubleshooting procedure will normally isolate a failure down to the few ICs that could be involved in the circuit failure. Checking the various nodes (branches common to one or more inputs and one or more outputs) is part of this procedure. The following series of steps will serve to locate most faulty ICs.

1. Refer to the appropriate data book(s) for the pin-out and diagram of the IC(s) under test.

2. Use the logic pulser to stimulate the inputs, while using the logic probe or logic clip to observe the response at the outputs. Make a note of each node that fails to respond to the stimulus, in the manner predicted by the truth table. The logic clip is especially useful for counters. (The term "node" is used to emphasize the fact that the failure of an IC to respond properly may be due to short-circuited tracks, or other failures external to the IC under test.)

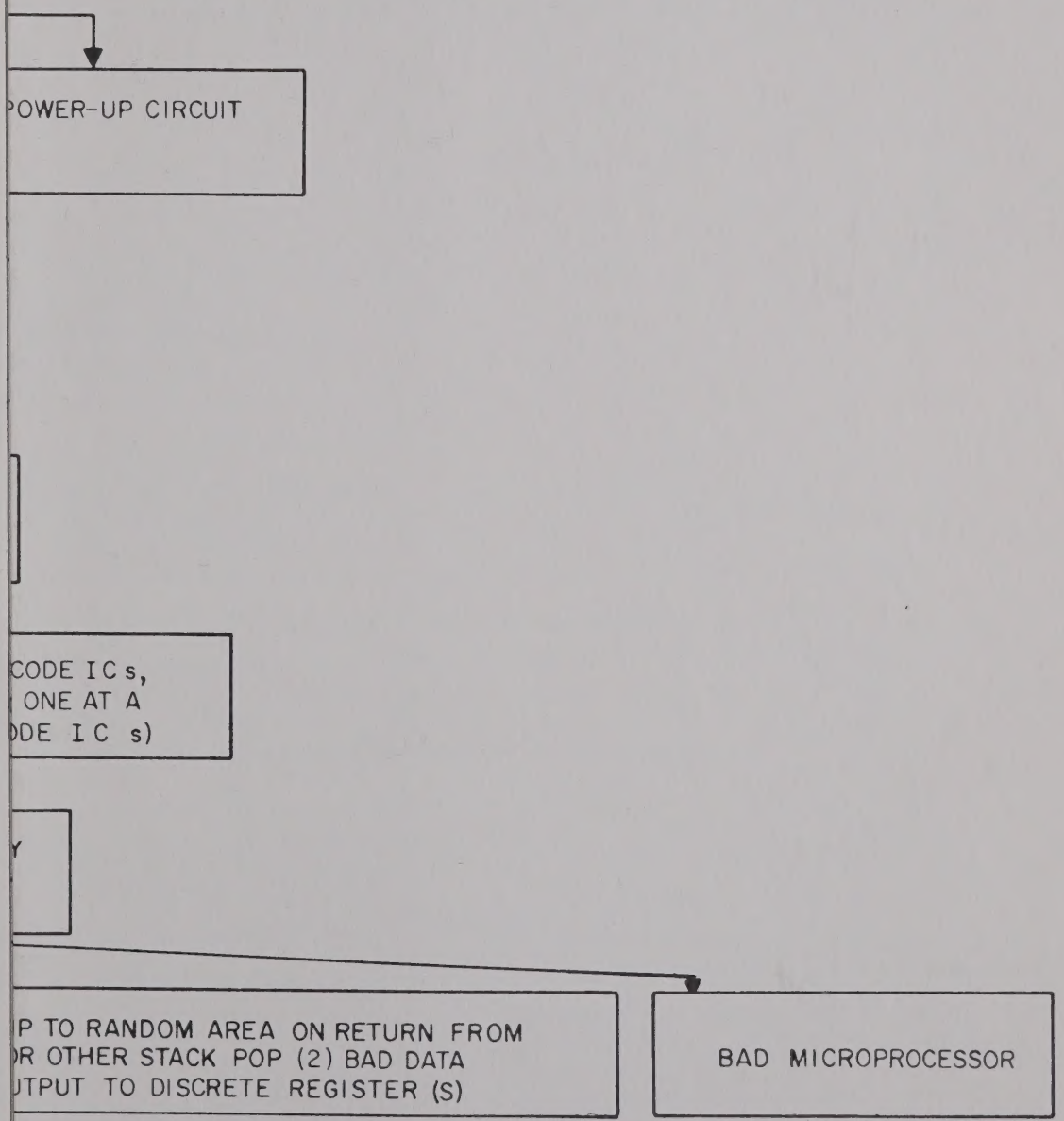

Figure 1-15. WJ-8718/232 Option Troubleshooting Tree

will often have the same effect as a high level on the input of the next IC in the circuit.

3. Short Circuit between Input and Ground or Vcc - If the input is shorted to ground, the device will react as through the input were low. If the input is shorted to Vcc, the device will react as though the input were high. Remember that either of these conditions can affect the output of the stage prior to this.

   A digital voltmeter (DVM) or oscilloscope can be used to distinguish between normal logic levels, and ground or Vcc. The logic pulser cannot override the Vcc or ground potential.

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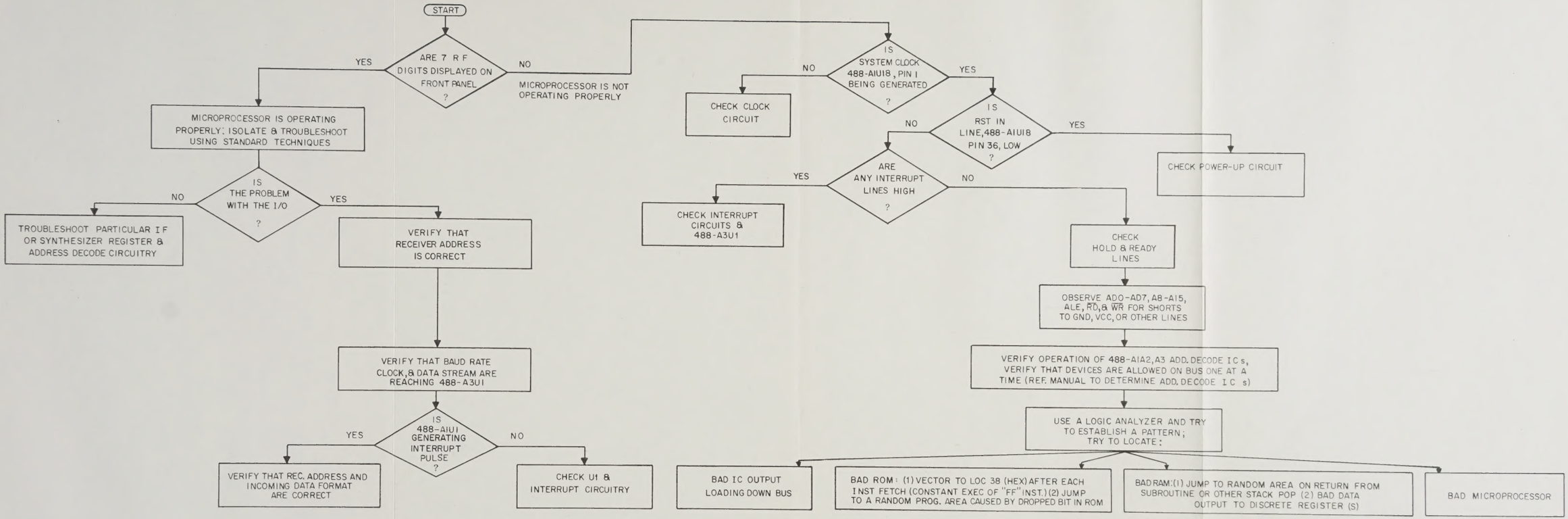

START
ARE 7 R F DIGITS DISPLAYED ON FRONT PANEL ?
YES
NO
MICROPROCESSOR IS NOT OPERATING PROPERLY
MICROPROCESSOR IS OPERATING PROPERLY; ISOLATE & TROUBLESHOOT USING STANDARD TECHNIQUES
IS THE PROBLEM WITH THE I/O ?
NO
YES
TROUBLESHOOT PARTICULAR I F OR SYNTHESIZER REGISTER & ADDRESS DECODE CIRCUITRY
VERIFY THAT RECEIVER ADDRESS IS CORRECT
VERIFY THAT BAUD RATE CLOCK, & DATA STREAM ARE REACHING 488-A3U1
IS 488-A1U1 GENERATING INTERRUPT PULSE ?
YES
NO
VERIFY THAT REC. ADDRESS AND INCOMING DATA FORMAT ARE CORRECT
CHECK U1 & INTERRUPT CIRCUITRY
IS SYSTEM CLOCK 488-A1U18, PIN 1 BEING GENERATED ?
NO
YES
CHECK CLOCK CIRCUIT
IS RST IN LINE, 488-A1U18 PIN 36, LOW ?
NO
YES
CHECK POWER-UP CIRCUIT
ARE ANY INTERRUPT LINES HIGH ?
YES
NO
CHECK INTERRUPT CIRCUITS & 488-A3U1
CHECK HOLD & READY LINES
OBSERVE AD0-AD7, A8-A15, ALE, RD, & WR FOR SHORTS TO GND, VCC, OR OTHER LINES
VERIFY OPERATION OF 488-A1A2, A3 ADD. DECODE IC s, VERIFY THAT DEVICES ARE ALLOWED ON BUS ONE AT A TIME (REF. MANUAL TO DETERMINE ADD. DECODE I C s)
USE A LOGIC ANALYZER AND TRY TO ESTABLISH A PATTERN; TRY TO LOCATE:
BAD IC OUTPUT LOADING DOWN BUS
BAD ROM: (1) VECTOR TO LOC 38 (HEX) AFTER EACH INST FETCH (CONSTANT EXEC OF "FF" INST.) (2) JUMP TO A RANDOM PROG. AREA CAUSED BY DROPPED BIT IN ROM
BAD RAM: (1) JUMP TO RANDOM AREA ON RETURN FROM SUBROUTINE OR OTHER STACK POP (2) BAD DATA OUTPUT TO DISCRETE REGISTER (S)
BAD MICROPROCESSOR

Figure 1-15. WJ-8718/232 Option Troubleshooting Tree

NOTE

When an IC fails, it usually fails completely. Thus, it is not normally necessary to observe the timing of the output signals. If an IC performs correctly under static test, it can be assumed to be good.

3. When one or more failing nodes have been located, use the logic probe to check the output of the IC that is driving the node. The logic probe will indicate a faulty level by showing a dim light. If a faulty level is indicated, the IC driving the node should be replaced.

4. Check for a short circuit to ground or Vcc by placing both the logic probe and logic pulser on the terminal. The logic pulser can override normal TTL output levels, but cannot override power supply potentials. Therefore, the presence of a pulse indicates that the node is not short circuited, and the absence of a pulse indicates the node is shorted to Vcc (if it is high) or to ground (if it is low). If a short circuit is indicated, proceed to step 5. If no short circuit to ground or Vcc is indicated, proceed to step 6.

5. A node short-circuited to ground or Vcc could be the result of either a short-circuited track on the board or an internal short in an IC. First, examine all branches of track connected to the node with the current tracer. Use the current tracer to isolate a defective IC: the circuit that draws the most current is generally defective.

6. If neither an open output (step 3), nor a node shorted to ground or Vcc (step 4) is indicated, look for a short between two nodes. This can be done more easily by turning OFF the unit's power, and using an ohmmeter to test for continuity between nodes that should not be common. (Refer to the schematic diagrams.) If a short circuit between nodes is indicated, proceed to step 7. If a short circuit is not evident, proceed to step 8.

7. The most probable cause of a short circuit between two nodes is a solder bridge on the board. If the two nodes which are short-circuited are connected to the same IC, the short circuit might be internal to the IC. If no external short circuit can be found, replace the common IC.

8. When open outputs and short circuits have been eliminated, the problem could be an open input on the IC being driven from the node, an internal IC failure, or an open signal path. The current tracer, or an ohmmeter, can be useful in finding an open signal path. For an opened input or an internal failure, the IC must be replaced.

1.8.5 REPAIR

1.8.5.1 General Repair Procedure

When a trouble has been isolated to a specific circuit board or assembly, the user may decide to make the repair himself or return the board or assembly to the factory for replacement or repair. After a repair has been made, alignment should be carried out, if necessary, and appropriate tests should be performed to verify proper operation.

1.8.5.2 Removing/Replacing Printed Circuit Components

Be careful not to damage the track when removing components from a printed circuit board. The soldering iron power should be no more than 40 watts, and a solder sipper or wicking procedure should be employed when removing solder. Noncorrosive soldering flux should be used when removing solder by wicking.

Removal of transistors which are soldered into printed circuit boards should be done with extra care. If the soldering iron is left on the wire lead of a transistor, heat travels up the wire and deforms the junction to which it is connected, destroying the transistor. To help prevent this, the transistor wire lead should be gripped, with a copper heat-sink or clamp, between the soldered joint and the transistor so that heat travelling up the wire will be transferred to the clip rather than the transistor.

Care must be taken so that an electrostatic difference of potential does not build up between transistors in a circuit and the soldering iron. The difference of potential can be reduced by touching the iron tip to a grounded point on the equipment just before soldering to another point in the circuit. Never solder transistorized equipment while it is operating.

Some soldering irons have ac flowing in a hairpin-shaped tip. The magnetic field from this hairpin can induce voltages into transistor circuits that can burn out transistors.

Power transistors may have their cases bolted to a heat sink metal, but they often require insulation between the case and heat sink. A thin piece of mica coated with special silicon grease to improve heat conduction through it may be used. A resistance check should always be made to make sure the case and heat sink are insulated from each other.

In returning components to the board, make sure that the holes are clear and be careful that the leads do not catch the edge of the track and lift it from the board. A good grade of resin core 60/40 solder should be used. Heat no longer than is necessary to achieve a good joint and use a heat sink where possible.

When replacing CMOS integrated circuits, use a low power soldering iron. To avoid static charge buildup, do not handle CMOS integrated circuits with the fingers.

1.9 REPLACEMENT PARTS LIST AND SCHEMATIC DIAGRAMS

The following list of manufacturers, parts lists, and schematic diagrams are intended as a supplement to the WJ-8718 Instruction Manual, and are to be used in conjunction with the applicable sections of that manual.

Mfr. Code	Name and Address
00779	AMP, Inc. 2800 Fulling Mill P.O. Box 3608 Harrisburg, PA 17105
01295	Texas Instruments, Inc. Semiconductor Group 13500 N. Central Expressway P.O. Box 225012 MIS 49 Dallas, TX 75265
01686	RCL Electronics/Shallcross, Inc. Subdivision of Hirsch and Associates, Inc. 195 McGregor St. Manchester, NH 03102
02660	Bunker Ramo-Eltra, Corp. Amphenol Division 2801 S. 25th Ave. Broadview, IL 60153
02735	RCA Corporation Solid State Division Route 202 Sommerville, NJ 08876
04713	Motorola, Inc. Semiconductor Products Sector 5005 E. McDowell Road Phoenix, AZ 85008
06776	Robertson-Nugent, Inc. 800 E. 8th St. P.O. Box 1208 New Albany, IN 47150
09021	Airco, Inc. Airco Electronics Bradford, PA 16701
14632	Watkins-Johnson Co. CEI Division 700 Quince Orchard Rd. Gaithersburg, MD 20878
19209	General Electric Co. Battery Business Dept. 441 Hwy N. P.O. Box 861 Gainesville, FL 32602
27014	National Semiconductor Corp. 2900 Semiconductor Drive Santa Clara, CA 95051
34649	Intel Corp. 3065 Bowers Ave. Santa Clara, CA 95051
56289	Sprague Electric Co. 87 Marshall St. North Adams, MA 01247
71279	Midland-Ross Corp. Cambion Division One Alewife Place Cambridge, MA 02140
75037	Minnesota Mining and Mfg. Co. Electro Products Division 3M Center St. Paul, MN 55101
73138	Beckman Industrial Corp. Beckman Electronic Technologies 2500 Harbor Blvd. Fullerton, CA 92634
80131	Electronic Industries Assoc. Washington, DC 20006
81349	Military Specifications

1.10 **TYPE WJ-8718/488-2 IEEE 488-2 INTERFACE OPTION**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
488-A1	Synthesizer, Interface	1	794275-X	14632	
488-A2	IF Interface	1	794308	14632	
488-A3	IO Interface	1	796075	14632	
488-J1	Connector, Receptacle, Multipin	1	57-20240-2	02660	
488-P1	Connector, Plug, Multipin	3	3332-0000	75037	
488-P2	Same as 488-P1				
488-P3	Same as 488-P1				
488-P4	Connector, Plug, 24 Pin	1	2-87456-0	00779	
488-P5	Connector, Plug, 3 Pin	1	87499-5	00779	
—	Contact Pin	25	87309-9	00779	
488-W1	Cable Assembly	1	288097-3	14632	
488-W2	Cable Assembly	1	380095-1	14632	

1.10.1 **TYPE 794275-X SYNTHESIZER INTERFACE AND MEMORY** REF DESIG **488-A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
BT1	Battery, Nickel-Cadmium: 2.4 V	1	41B901BD16-1	19209	
CR1	Diode	2	1N4449	80131	93332
CR2	Same as CR1				
C1	Capacitor, Ceramic, Disc: .1 µF, 20%, 100 V	5	8131M100-651-104M	59660	
C2 Thru C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	2	196D226X0015KE3	56289	
C7	Same as C6				
C8*	Capacitor, Ceramic, Disc: 680 pF, 5%, 100 V, NPO	1	8121-100-C0G0-681J	59660	
C9	Capacitor, Ceramic, Disc: 47 µF, 20%, 50 V, Z5U	1	34452-1	14632	
C10	Capacitor, Polycarbonate: 1 µF, 10%, 30 V	1	ECR105AK	50558	
C11	Same as C1				
C12	Same as C1				
Q1	Transistor	1	2N3251	80131	04713
R1	Not Used				
R2	Resistor, Fixed, Film: 820 Ω, 5%, 1/4 W	1	CF1/4-820 OHMS/J	09021	
R3	Resistor, Fixed, Film: 82 kΩ, 5%, 1/4 W	2	CF1/4-82K/J	09021	
R4	Resistor, Fixed, Film: 150 Ω, 5%, 1/4 W	1	CF1/4-150 OHMS/J	09021	
R5	Resistor, Fixed, Film: 390 Ω, 5%, 1/4 W	1	CF1/4-390 OHMS/J	09021	
R6	Same as R3				
R7	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	6	CF1/4-10K/J	09021	
R8	Same as R5				
R9	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	5	CV1/4-1K/J	09021	
R10 Thru R13	Same as R9				
R14	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/4W	1	CF1/4-3.3K/J	09021	
R15 Thru R19	Same as R7				
U1	Integrated Circuit	1	32732**	14632	
U2	Not Used				
U3	Integrated Circuit	1	841093	14632	
U4	Integrated Circuit	1	MD74SC245AC	36665	
U5	Integrated Circuit	2	MD74SC374AC	36665	
U6	Same as U5				
U7	Integrated Circuit	2	MD74SC138AC	36665	
*	Nominal value, final valve factory selected.				
**	For ordering software, refer to the numbered label on the IC.				

REF DESIG **488-A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U8	Same as U7				
U9	Integrated Circuit	1	MM74PC00N	27014	
U10	Integrated Circuit	1	SN74LS09N	01295	
U11	Integrated Circuit	1	SN74LS14N	01295	
U12	Integrated Circuit	5	MM74C374N	27014	
U13 Thru U16	Same as U12				
U17	Not Used				
U18	Integrated Circuit	1	P8085A	34649	
VR1	Diode, Zener: 8.2 V Silicon	1	1N756A	80131	04713

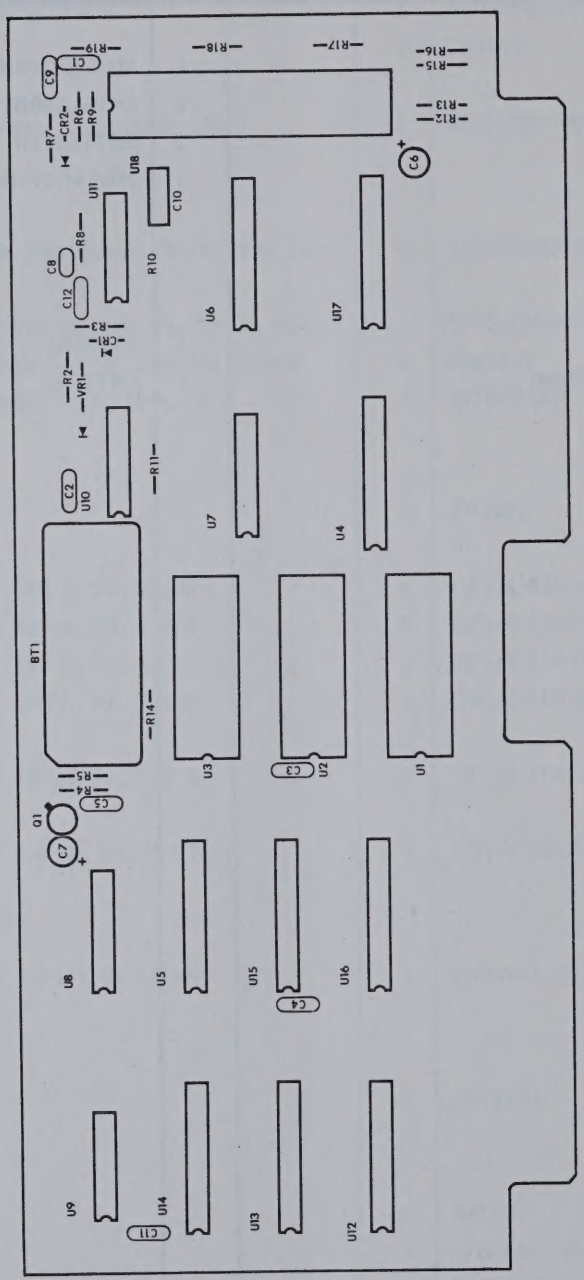


Figure 1-16. Type 794275-X Synthesizer Interface/Memory (488-A1) Location of Components

1.10.2 **TYPE 794308-1 IF INTERFACE** REF DESIG **488-A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	3	1N4449	80131	93332
CR2	Same as CR1				
CR3	Same as CR1				
C1	Capacitor, Ceramic, Disc: .1 µF, 20%, 50 V	9	34475-1	14632	
C2 Thru C5	Same as C1				
C6	Capacitor, Ceramic, Monolithic: 220 pF, 5%, 100 V	1	8121-100-C0G0-221J	59660	
C7	Same as C1				
C8	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	2	196D1869020KE3	56289	
C9	Same as C8				
C10	Same as C1				
C11	Same as C1				
C12	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	1	196D226X0015KE3	56289	
C13	Not Used				
C14	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D47X0035JE3	56289	
C15	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	1	196D476X0020PE4	56289	
C16	Same as C1				
C17	Capacitor, Ceramic, Disc: .47 µF, 20%, 50 V, Z5U	1	34452-1	14632	
E1-E2	Terminal, Forked	2	140-1941-02-01	71279	
J1	Connector, Receptacle, 40 Pin	1	1-87567-6	00779	
J2	Connector, Receptacle, 16 Pin	3	87567-4	00779	
J3	Same as J2				
J4	Same as J2				
RN1	Resistor, Network	3	765-1-R10K	73138	
RN2	Same as RN1				
RN3	Resistor, Network	1	4308R-101-103	73138	
RN4	Same as RN1				
R1	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	2	CF1/8-10K/J	09021	
R2	Resistor, Fixed, Composition: 22 Ω, 5%, 1/2 W	1	RCR20G220JS	81349	01121
R3	Resistor, Fixed, Composition: 2.7 kΩ, 5%, 1/4 W	1	RCR07G272JS	81349	01121
R4	Same as R1				
R5	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	2	CF1/4-1K/J	09021	
R6	Resistor, Fixed, Film: 100 Ω, 5%, 1/4 W	1	CF1/4-100 OHMS/J	09021	
R7	Resistor, Trimmer, Film: 20 kΩ, 10%, 1/2 W	1	62PAR20K	73138	
R8	Resistor, Fixed, Film: 12 kΩ, 5%, 1/4 W	1	CF1/4-12K/J	09021	
R9	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	6	CF1/4-10K/J	09021	
R10 Thru R13	Not Used				
R14	Resistor, Fixed, Film: 39 kΩ, 5%, 1/4 W	1	CF1/4-39K/J	09021	
R15	Same as R9				
R16	Resistor, Fixed, Film: 82 kΩ, 5%, 1/4 W	1	CF1/4-82K/J	09021	

REF DESIG PREFIX **488-A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R17	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/4 W	2	CF1/4-8.2K/J	09021	
R18	Same as R9				
R19	Same as R5				
R20	Same as R17				
R21	Same as R9				
R22	Resistor, Fixed, Film: 750 Ω, 5%, 1/4 W	1	CF1/4-750 OHMS/J	09021	
R23	Same as R9				
R24	Same as R9				
R25	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3K/J	09021	
U2	Same as U1				
U3	Integrated Circuit	2	MM74C244N	27014	
U4	Integrated Circuit	3	MM74C374N	27014	
U5	Same as U4				
U6	Same as U1				
U7	Same as U3				
U8	Integrated Circuit	1	MD74SC374AC	36665	
U9	Same as U4				
U10	Integrated Circuit	1	MM74PC00N	27014	
U11	Integrated Circuit	2	MM74PC138N	27014	
U12	Same as U11				
U13	Integrated Circuit	2	MM74PC32N	27014	
U14	Integrated Circuit	1	MM74PC04N	27014	
U15	Integrated Circuit	1	MM74PC08N	27014	
U16	Integrated Circuit	1	CD4066BE	02735	
U17	Integrated Circuit	1	MM74C173N	27014	
U18	Integrated Circuit	1	MM74C14N	27014	
U19	Same as U13				
U20	Integrated Circuit	1	MD74SC245AC	36665	
U21	Integrated Circuit	1	CD4013BE	02735	
U22	Integrated Circuit	1	MC14053BCP	04713	
U23	Integrated Circuit	1	DAC0830LCN	27014	
U24	Integrated Circuit	1	TL064CN	01295	
U25	Integrated Circuit	1	ADC0808CCN	27014	
VR1	Diode, Zener: 5.1 V Silicon	3	1N751A	80131	04713
VR2	Same as VR1				
VR3	Same as VR1				
XU1	Socket, Integrated Circuit	7	ICN-163-S3-T	06776	
XU2	Same as XU1				
XU3	Socket, Integrated Circuit	8	ICN-203-S3-T	06776	
XU4	Same as XU3				
XU5	Same as XU3				

REF DESIG **488-A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
XU6	Same as XU1				
XU7	Same as XU3				
XU8	Same as XU3				
XU9	Same as XU3				
XU10	Socket, Integrated Circuit	9	ICN-143-S3-T	06776	
XU11	Same as XU1				
XU12	Same as XU1				
SU13 Thru XU16	Same as XU10				
XU17	Same as XU1				
XU18	Same as XU10				
XU19	Same as XU10				
XU20	Same as XU3				
XU21	Same as XU10				
XU22	Same as XU1				
XU23	Same as XU3				
XU24	Same as XU10				
XU25	Socket, Integrated Circuit	1	ICN-286-S5-T	06776	

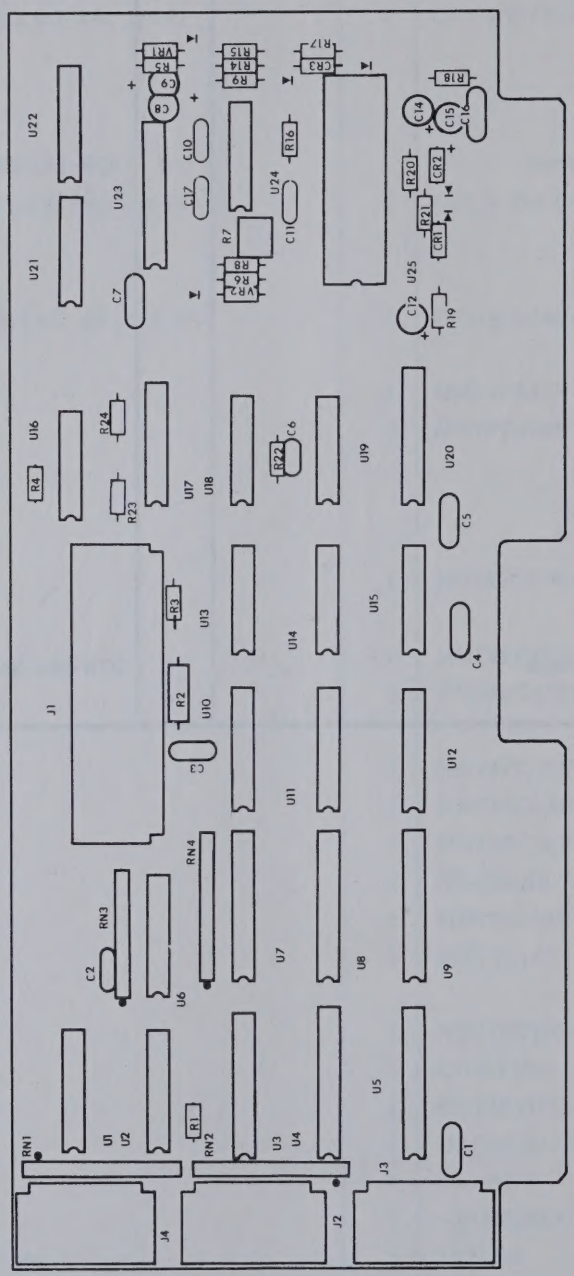


Figure 1-17. Type 794308-1 IF Interface (488-A2), Location of Components

1.10.3 **TYPE 796075 I/O INTERFACE** REF DESIG PREFIX **488-A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: .01 µF, 20%, 50 V	1	34453-1	14632	
C2	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	1	196D226X0015KE3	56289	
C3	Capacitor, Ceramic, Disc: .1 µF, 20%, 50 V	3	34475-1	14632	
C4	Same as C3				
C5	Same as C3				
J1	Connector, Receptacle, 24 Pin	1	87571-9	00779	
R1	Resistor, Fixed, Film: 43 OHMS, 5%, 1/4 W	1	CF1/4-43 OHMS/J	09021	
R2	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	1	CF1/4-10K/J	09021	
R3	Not Used				
R4	Not Used				
R5	Resistor, Fixed, Composition: 2.2 kΩ, 5%, 1/4 W	3	RCR07G222JS	81349	01121
R6	Same as R5				
R7	Same as R5				
S1	Switch, Dipped	1	PIP8	01686	
U1	Integrated Circuit	1	P8291A	34649	
U2	Integrated Circuit	1	SN75160N	01295	
U3	Integrated Circuit	1	SN75161N	01295	
U4	Integrated Circuit	1	DM81LS96N	27014	
U5	Resistor, Network	1	765-1-R10K	73138	
U6	Integrated Circuit	1	SN74LS273N	01295	
U7	Integrated Circuit	1	SN74LS138N	01295	
U8	Integrated Circuit	1	SN74LS14N	01295	
U9	Integrated Circuit	1	SN74LS32N	01295	
U10	Integrated Circuit	1	SN74LS74N	01295	
XU1	Socket/Integrated Circuit	1	ICN-406-S5-T	06776	
XU2	Socket/Integrated Circuit	4	ICN-203-S3-T	06776	
XU3	Same as XU2				
XU4	Same as XU2				
XU6	Same as XU2				
XU7	Socket/Integrated Circuit	1	ICN-163-S3-T	06776	
XU8	Socket, Integrated Circuit	1	ICN-143-S3-T	06776	

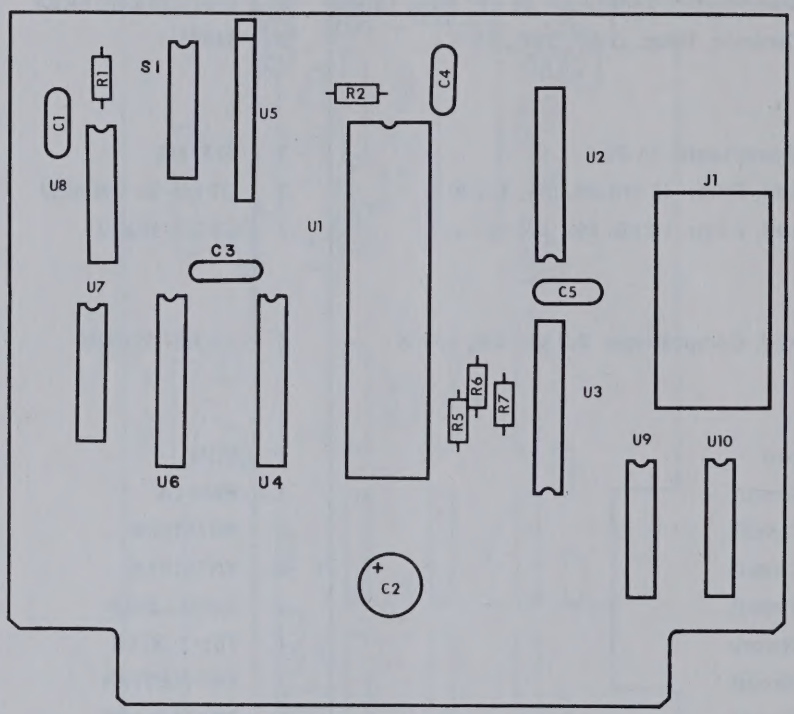


Figure 1-18 Type 796075 I/O Interface (488-A3), Location of Components

SCHEMATIC DIAGRAMS

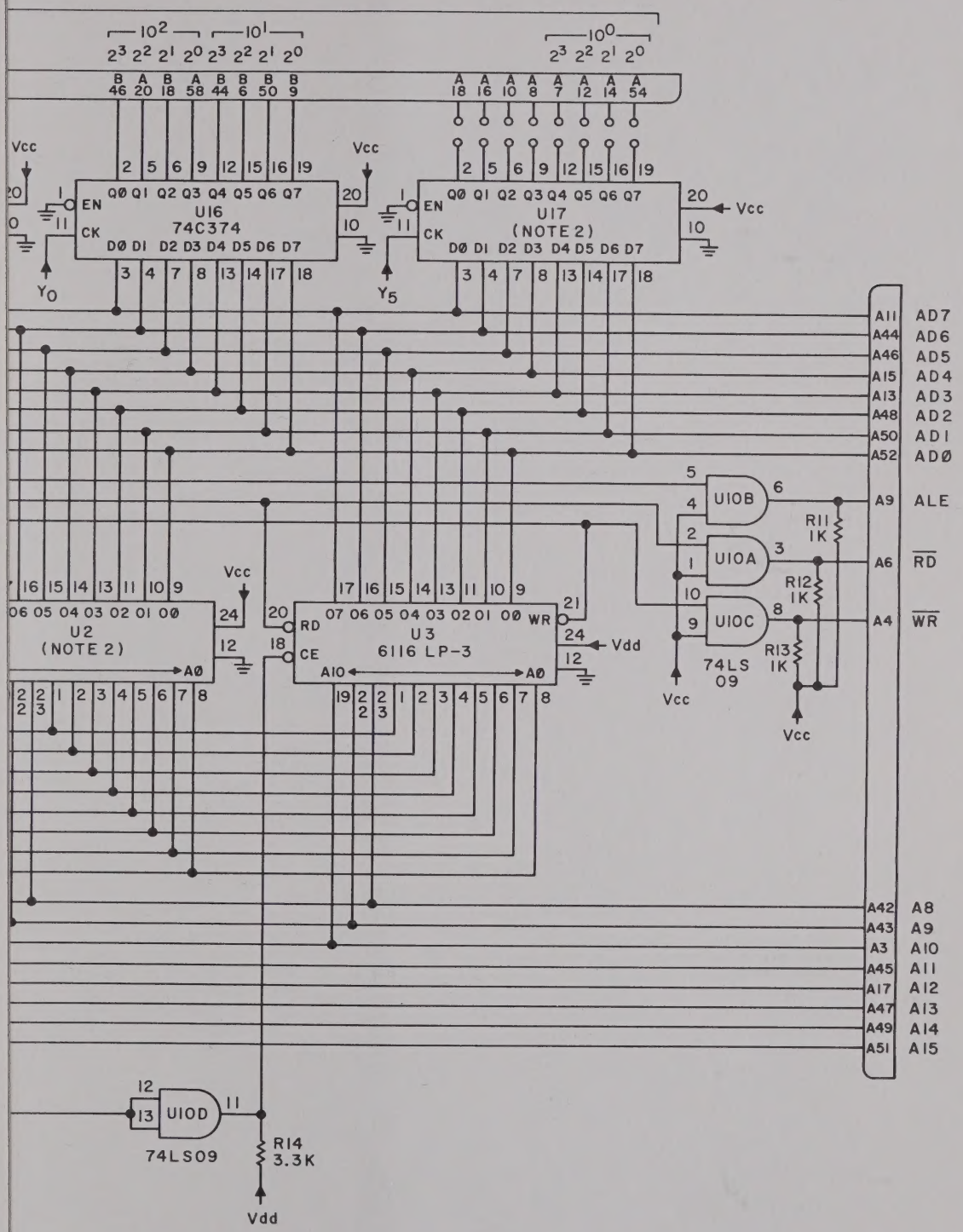
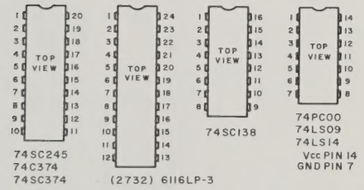


Figure 1-19. Type 794275-X Synthesizer Interface (488-A1), Schematic Diagram 570208

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN μF.
2. DIFFERENCE BETWEEN TYPE/IC NO.S IS LISTED IN TABLE.
3. NOMINAL VALUE. FINAL VALUE FACTORY SELECTED.

TYPE	U1	U2	U17	OPTION
794275-1	841089	N/U	N/U	8718/MFP
794275-2	841087-1	N/U	N/U	8718/M232
794275-3	841088-1	N/U	N/U	8718/M488-2
794275-4	841088-1	N/U	N/U	WJ-8718A/NAV/MFP



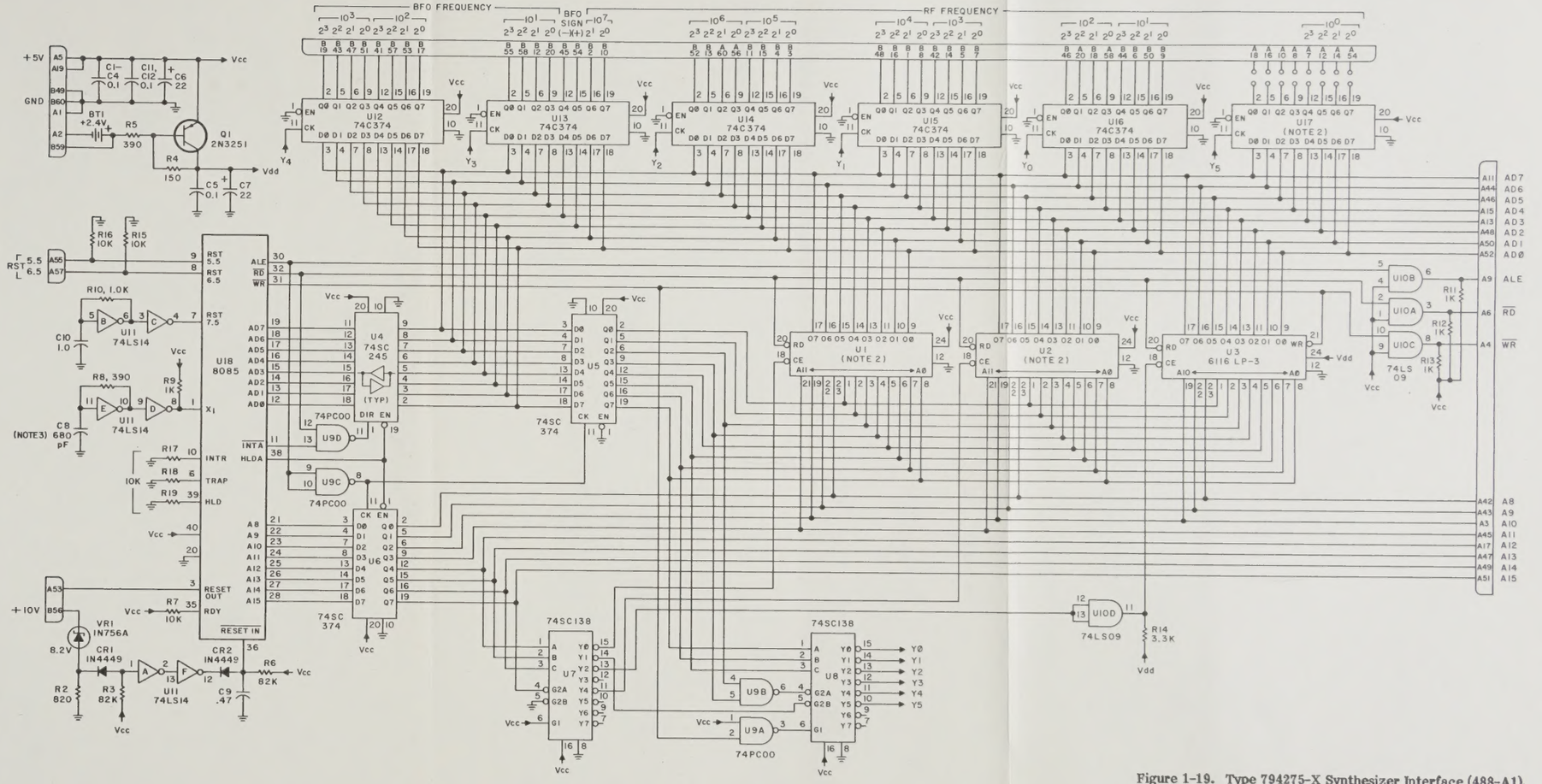
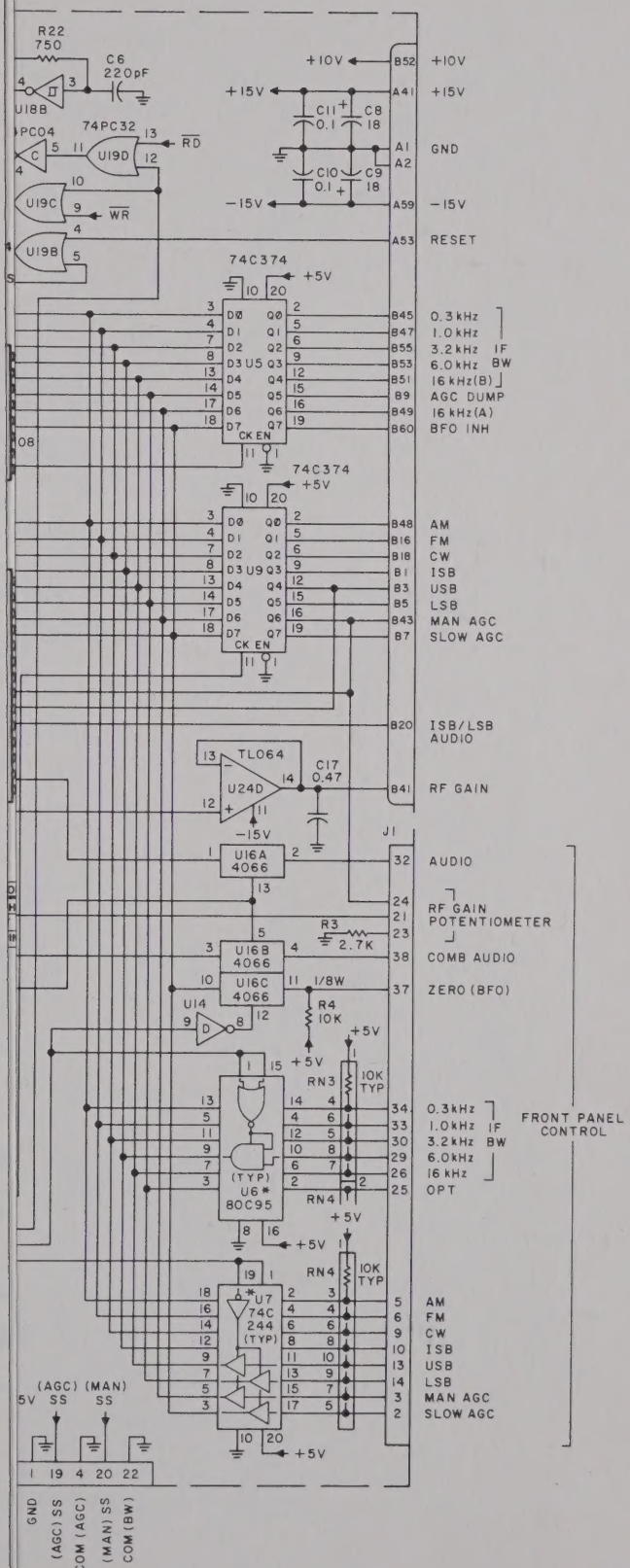
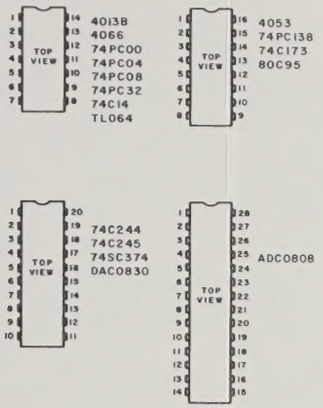


Figure 1-19. Type 794275-X Synthesizer Interface (488-A1), Schematic Diagram 570208



re 1-20. Type 794308-1 IF Interface (488-A2), Schematic Diagram 570239

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN µF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE.
3. FINAL VALUE FACTORY SELECTED.



TYPE	UNIT	COMPONENTS (*)	R25
794308-1	WJ-8718	AS SHOWN	AS SHOWN
794308-2	WJ-8718/MFP	OMIT IN FULL	JW1
794308-3	WJ-8718A/NAVMFP	OMIT IN FULL	JW1

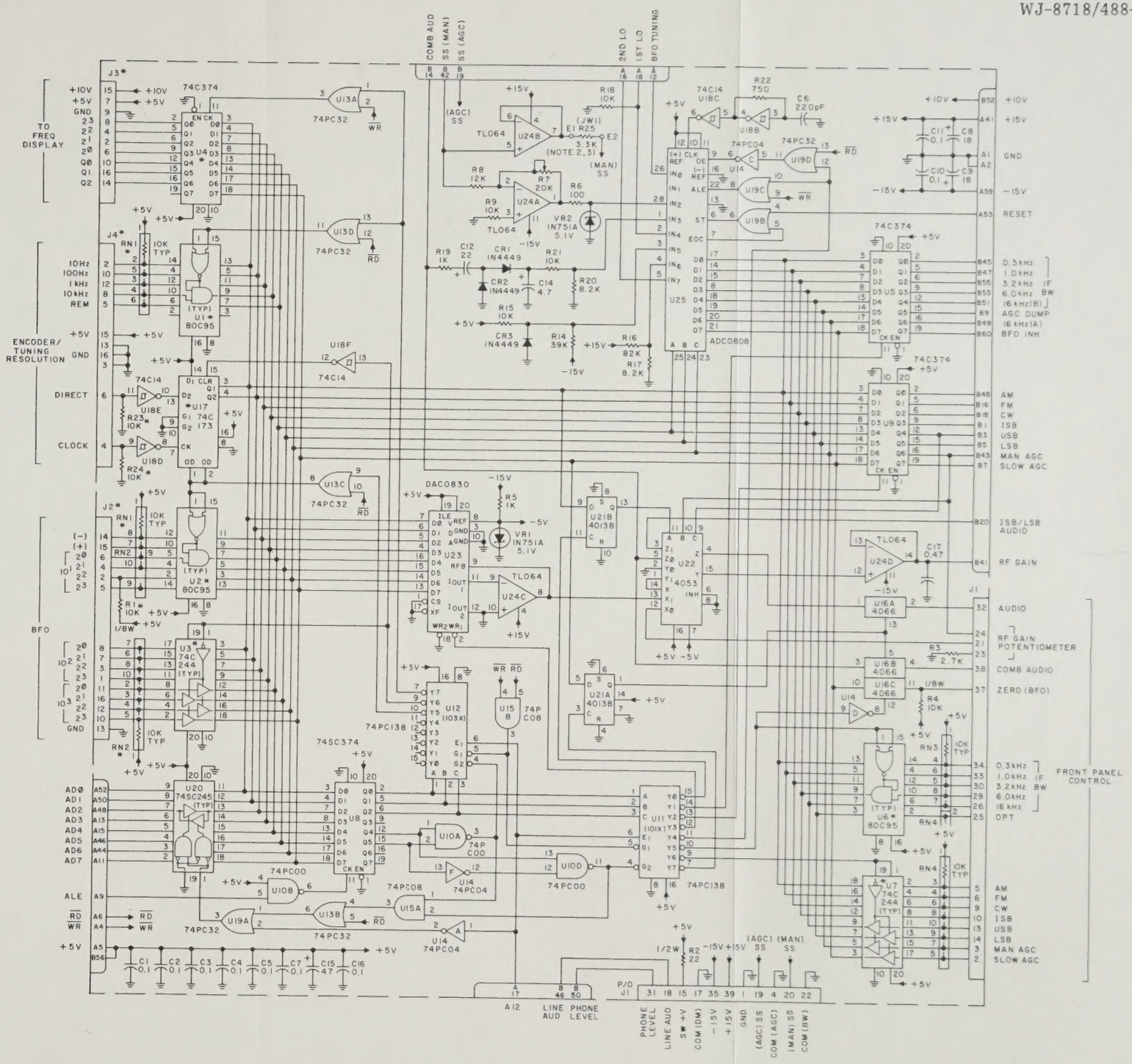


Figure 1-20. Type 794308-1 IF Interface (488-A2), Schematic Diagram 570239

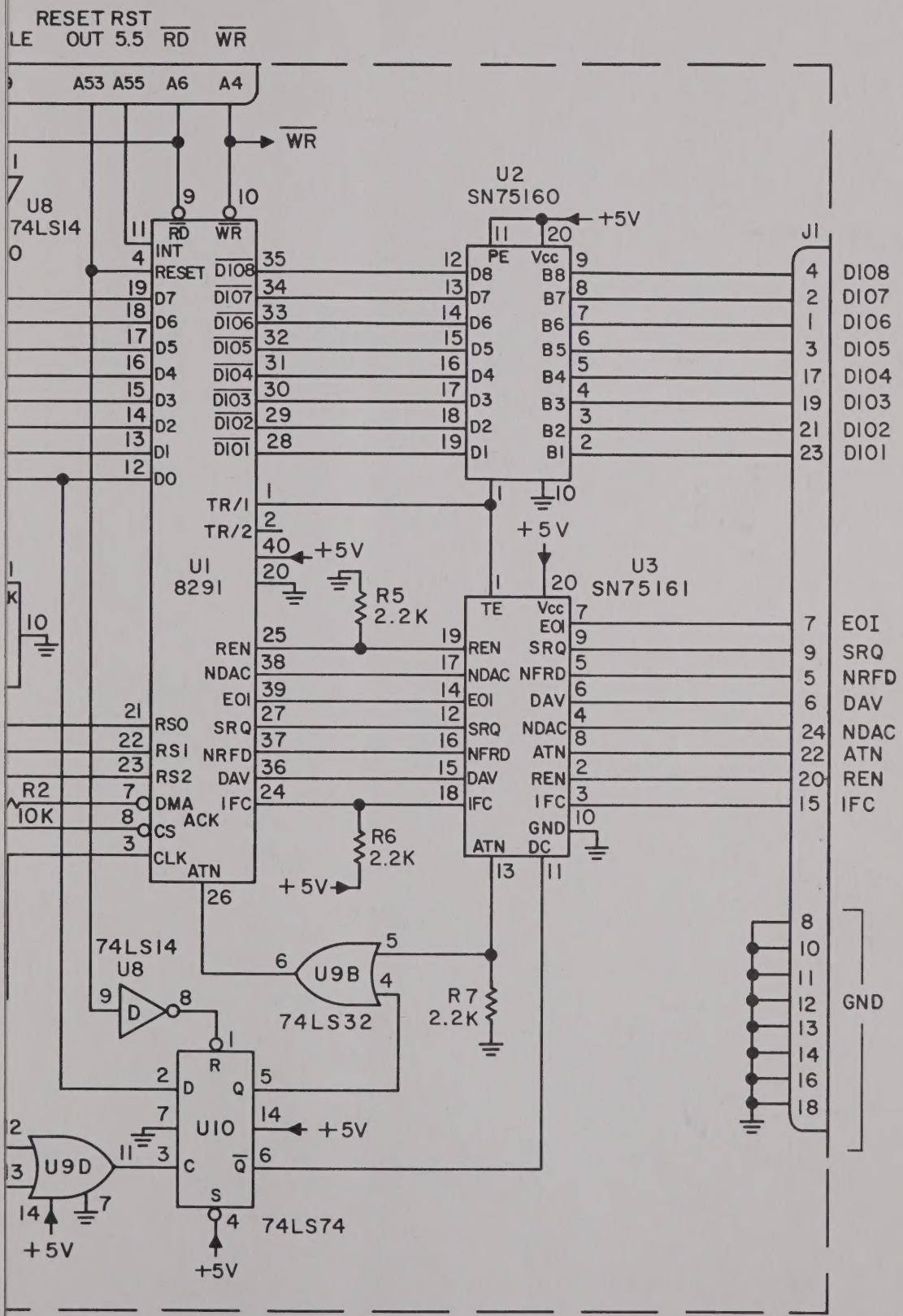
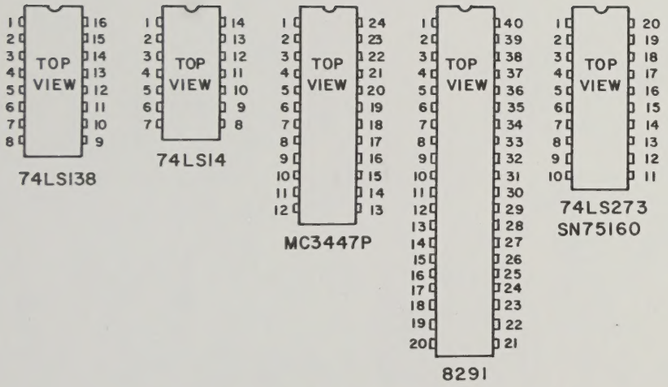


Figure 1-21. Type 796075 I/O Interface (488-A3), Schematic Diagram 480096

NOTES:

UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
b) CAPACITANCE IS IN µF.



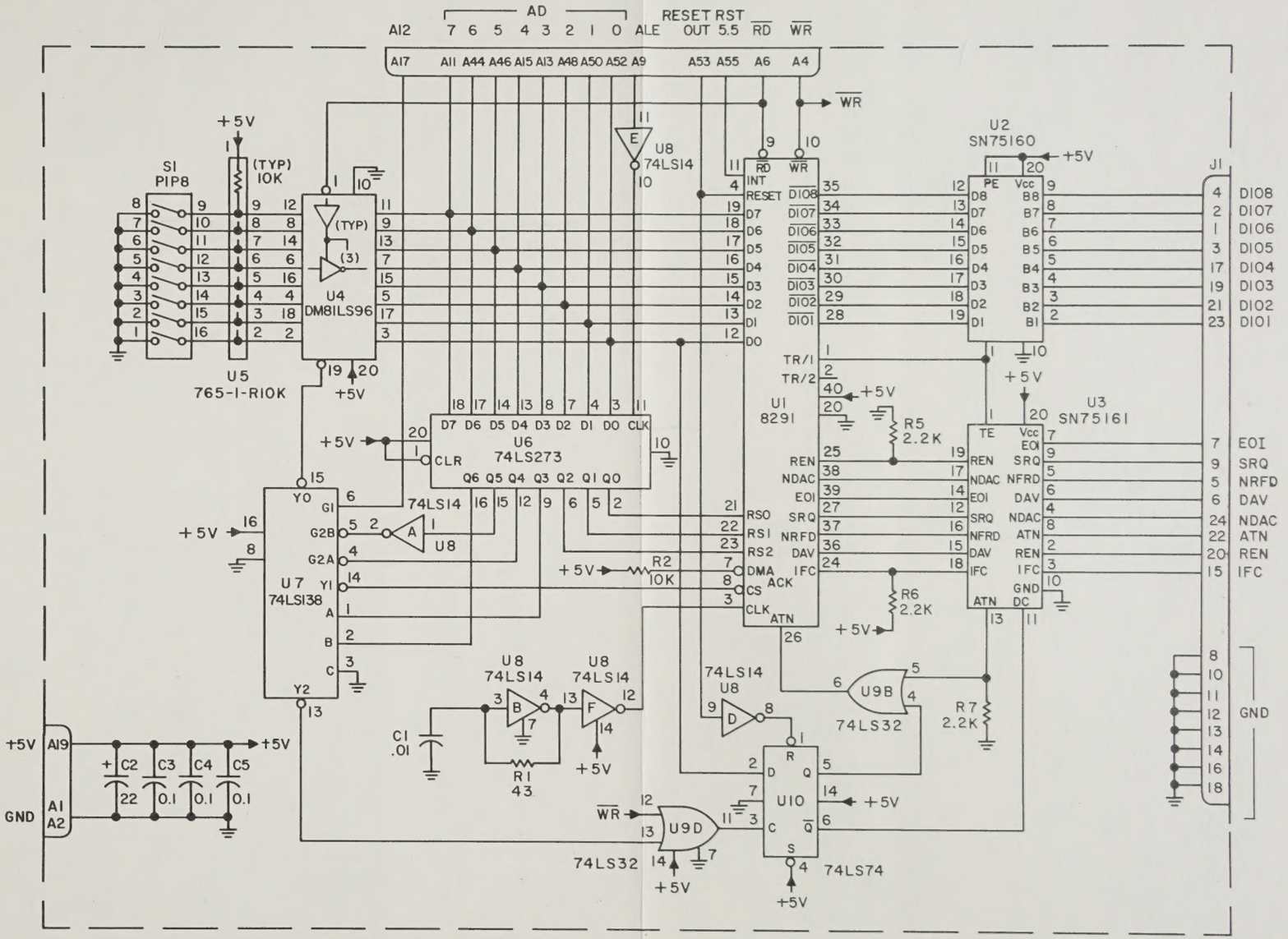


Figure 1-21. Type 796075 I/O Interface (488-A3), Schematic Diagram 480096

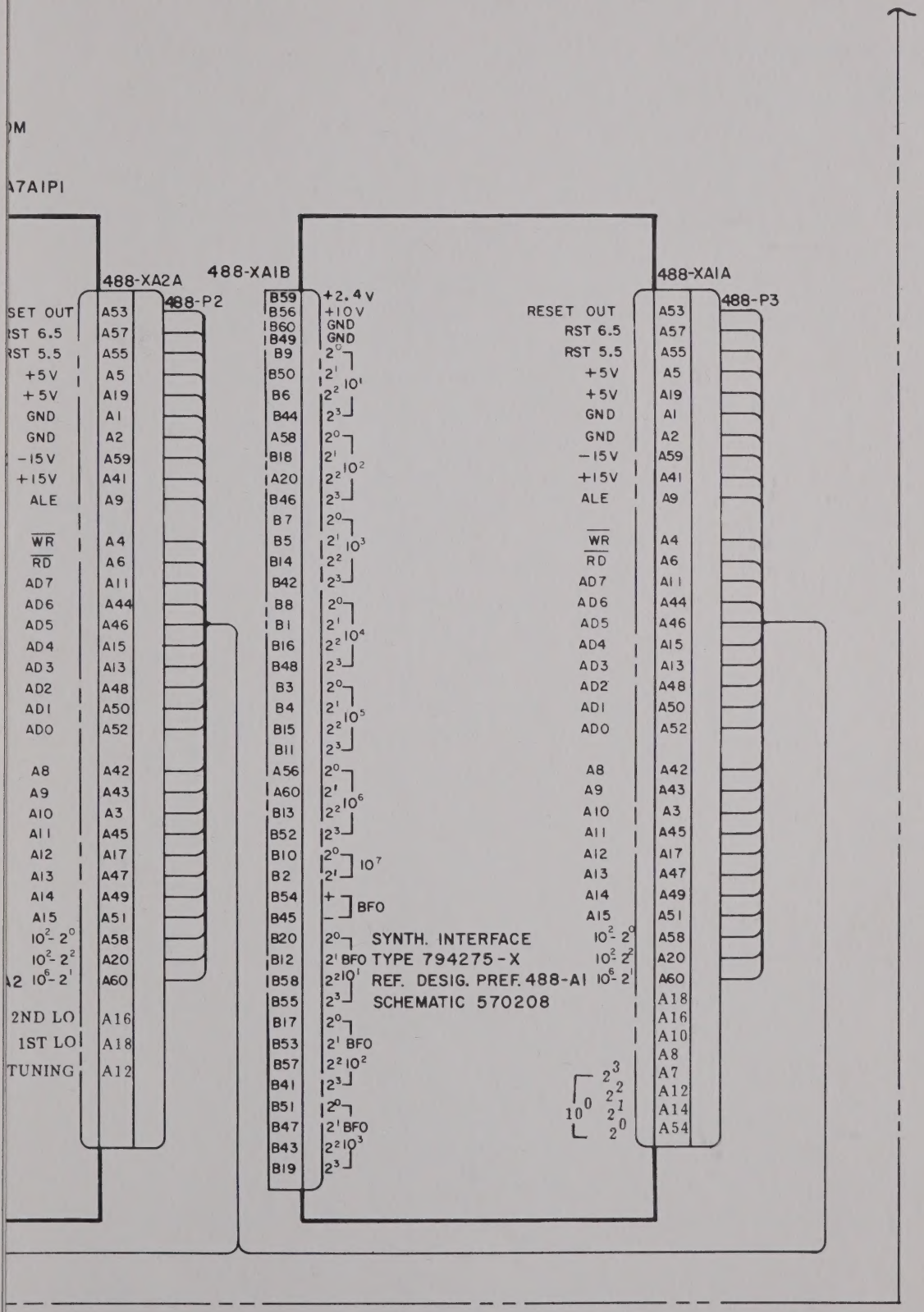


Figure 1-22. WJ-8718/488-2 Option, Schematic Diagram 480115

NOTES
1. PHANTOM LINES INDICATE PRE-EXISTING MODULES.
2. 488-A1 REPLACES A6A1, 488-A2 REPLACES A6A2 OF MAIN FRAME WHEN 8718/488 OPTION IS IMPLEMENTED.
3. 488-P1, 488-P2 & 488-P3 OF 488-W1 ARE WIRED PIN FOR PIN.

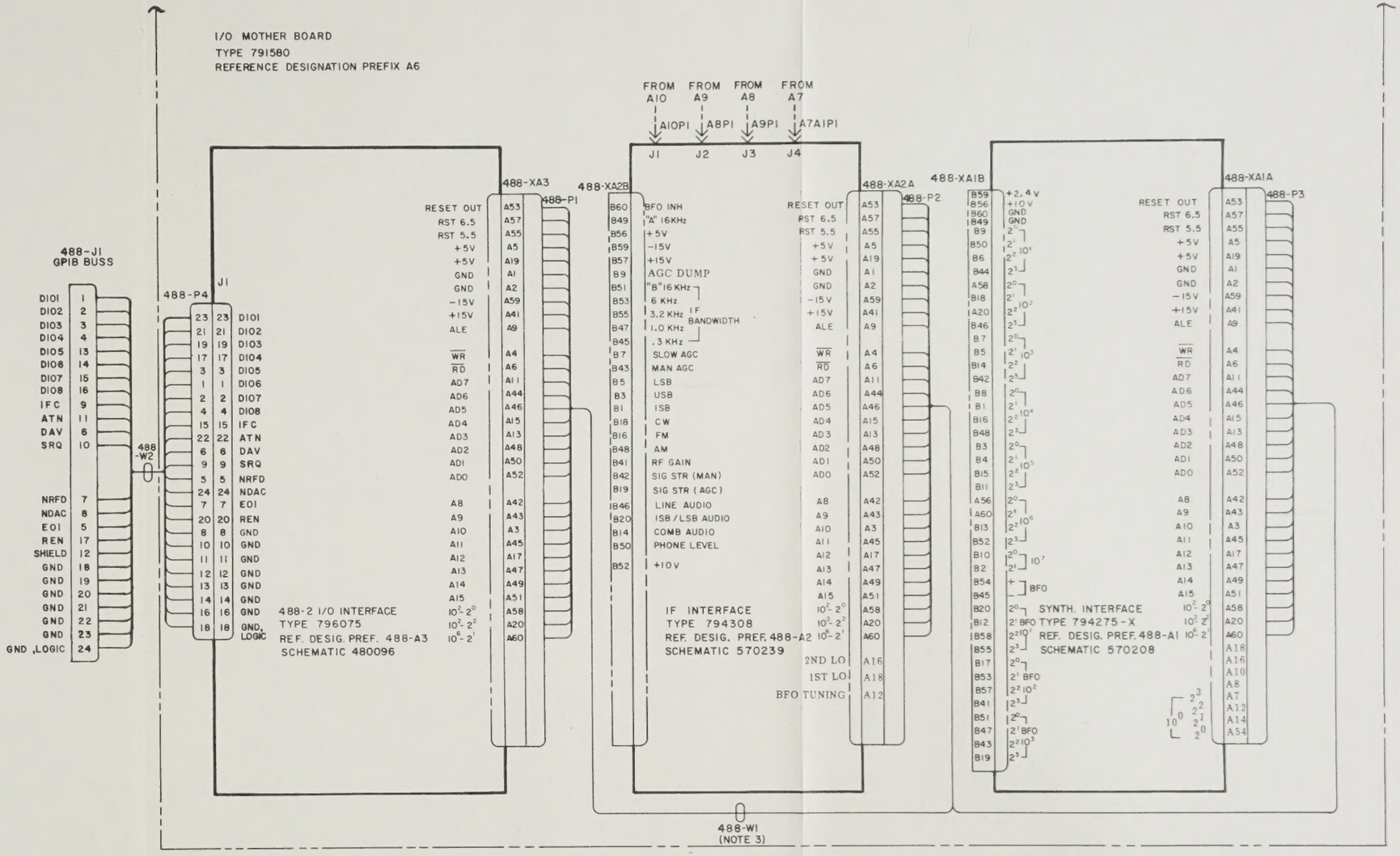


Figure 1-22. WJ-8718/488-2 Option, Schematic Diagram 480115